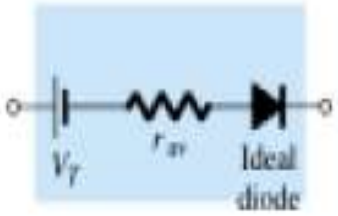
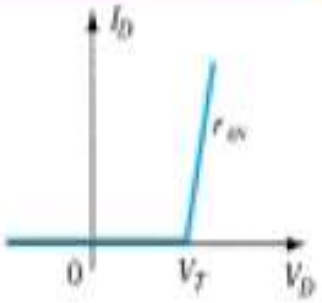
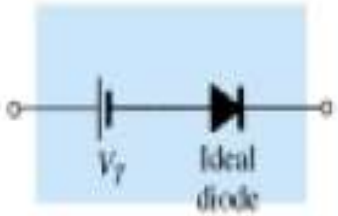
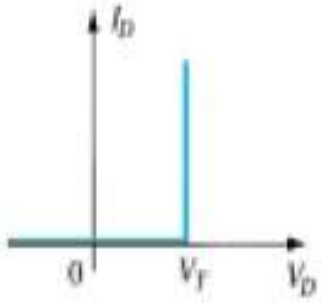
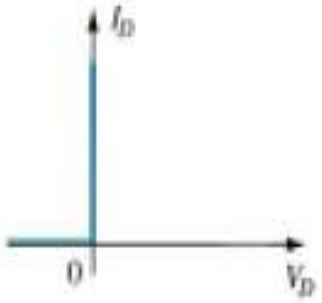
Lecture 7:

11. Diode Equivalence Circuits:

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating pregion.

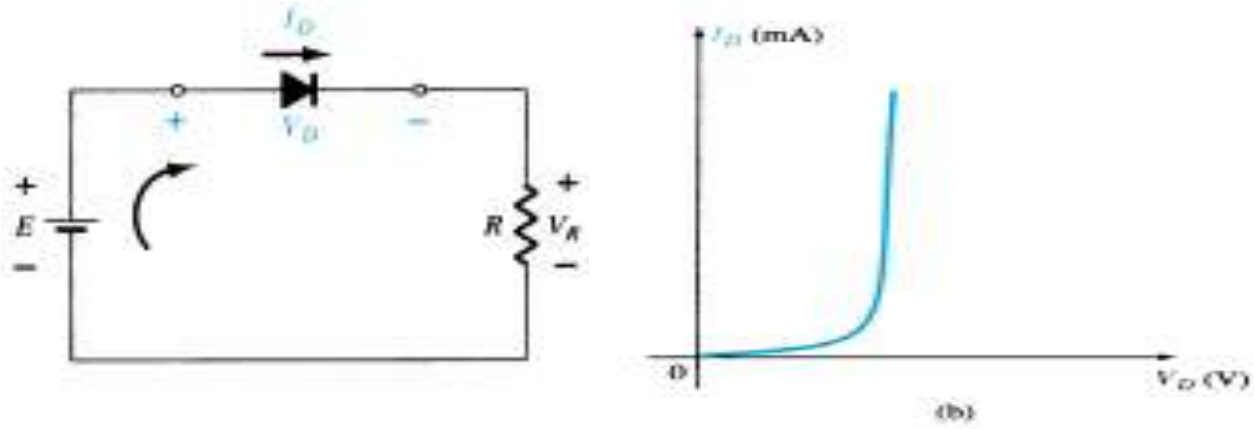
In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Type	*Conditions*	*Model*	*Characteristics*
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_T$		

Diode applications:

LOAD-LINE ANALYSIS:

The applied load will normally have an important impact on the point or region of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is, for obvious reasons, called *load-line analysis*.



(a) (b)

Fig (2-1) diode series configuration (a): circuit (b): characteristic

Applying Kirchhoff's voltage law to the series circuit of Fig. 2.1a will result in

$$E - V_D - V_R = 0$$

Or

$$E = V_D + I_D R$$ ……..eq (2.1)

If we *set VD* =0 V in Eq. (2.1) and solve for *ID*, we have the magnitude of *ID on* The vertical axis. Therefore, with *VD* =0 V, Eq. (2.1) becomes:

$$E = V_D + I_D R$$
$$= 0\ \text{V} + I_D R$$

And

$$I_D = \frac{E}{R}\bigg|_{V_D=0\ \text{V}}$$

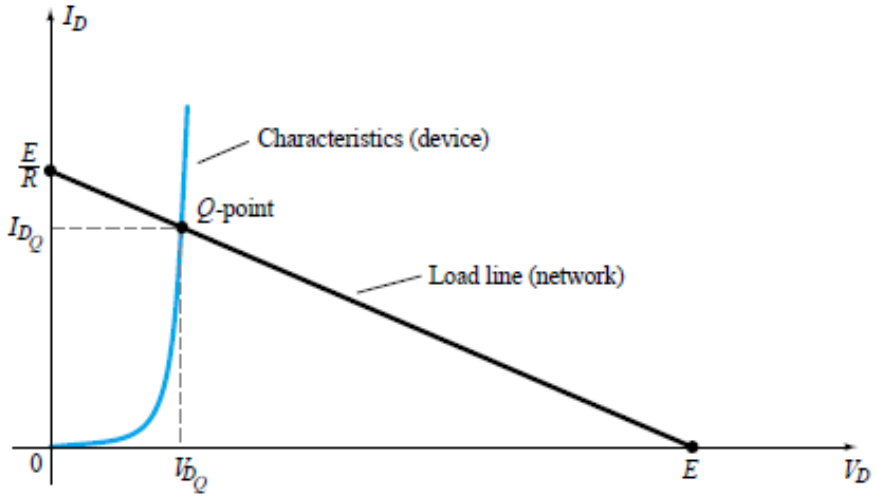


Fig (2-2)

As shown in Fig. 2.2. If we *set ID* =0 A in Eq. (2.1) and solve for *VD*, we have the Magnitude of *VD on* the horizontal axis. Therefore, with *ID* =0 A, Eq. (2.1) becomes

$$E = V_D + I_D R$$
$$= V_D + (0\ \text{A})R$$

And

$$V_D = E|_{I_D=0\ A}$$

Example(2.1):

For the series diode configuration of Fig. 2.3a employing the diode characteristics of Fig. 2.3b determine:
(a) *VDQ* and *IDQ*.
(b) *VR*.

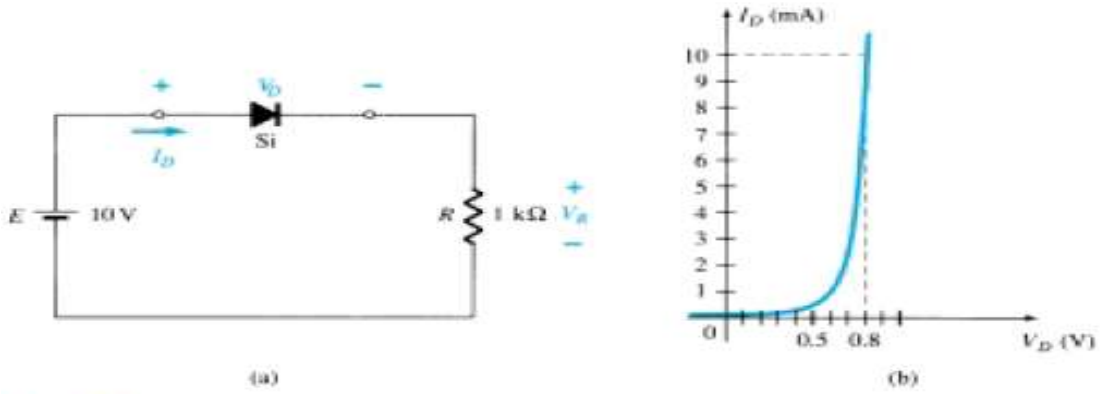


Figure 2.3 (a) Circuit; (b) characteristics.

Solution

(a) Eq. (2.2): $I_D = \left.\frac{E}{R}\right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{2\text{ k}\Omega} = 10\text{ mA}$

Eq. (2.3): $V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the *Q*-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$

$$I_{D_Q} \cong \mathbf{9.25\text{ mA}}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

(b) $V_R = I_R R = I_{D_Q} R = (9.25\text{ mA})(1\text{ k}\Omega) = \mathbf{9.25\text{ V}}$

or $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

The difference in results is due to the accuracy with which the graph can be read. Ideally, the results obtained either way should be the same.

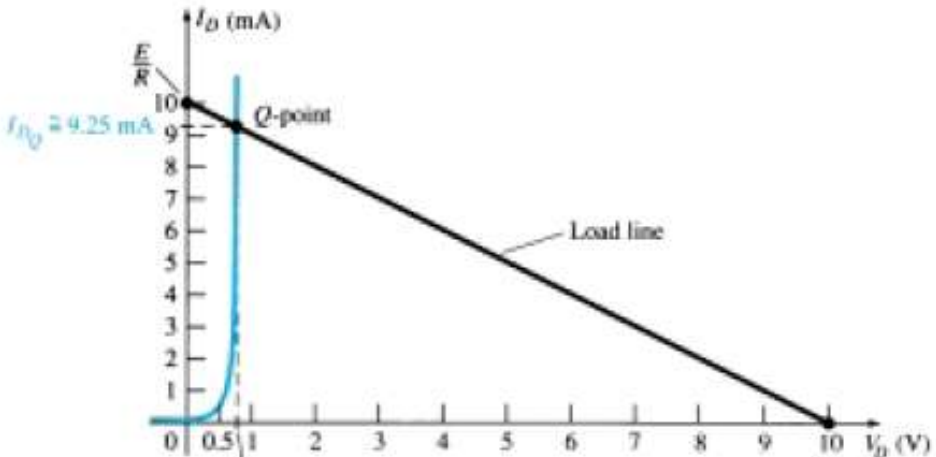
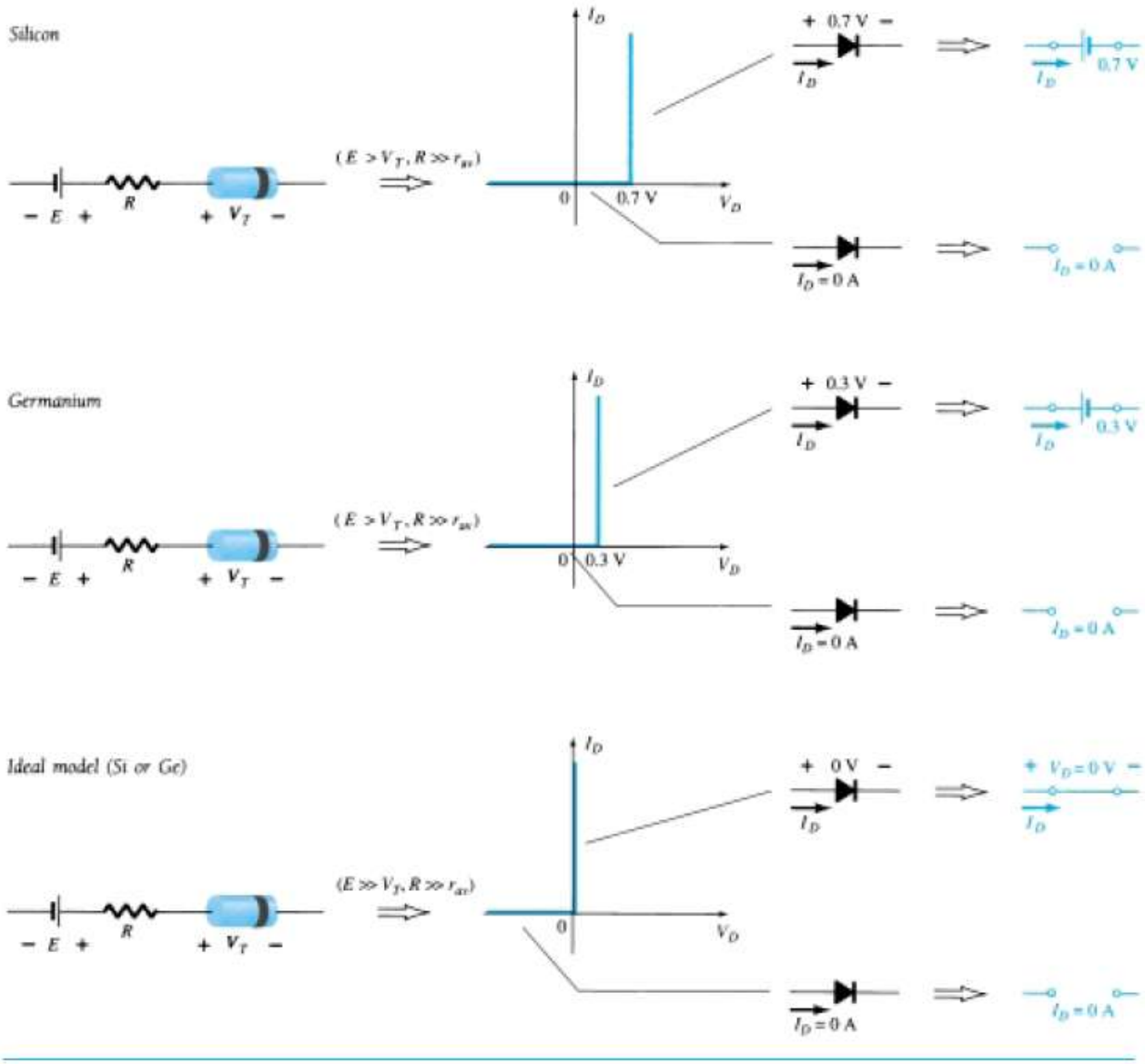


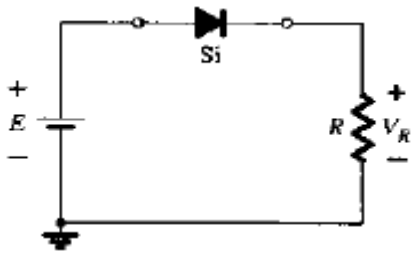
TABLE 2.1 Approximate and Ideal Semiconductor Diode Models



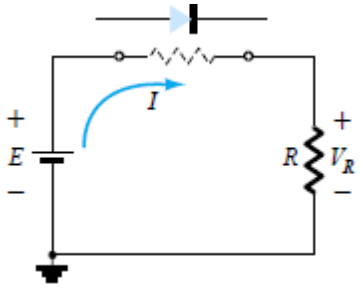
Lecture 8:

Series diode configurations with DC inputs

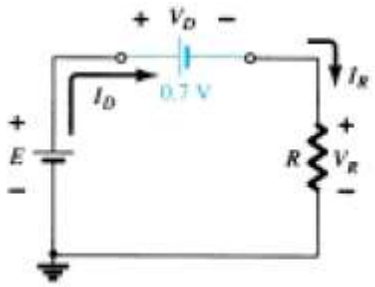
*In general, a diode is in the **on** state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and **VD≥ 0.7V** for silicon and **VD ≥ 0.3V** for germanium.*



(a)Series diode configuration



(b) Determining the state of diode of fig (a)

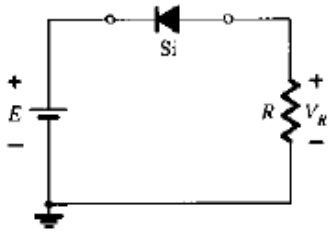


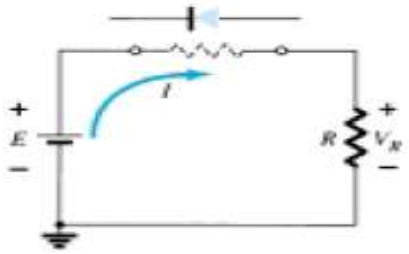
(C) Substituting the equivalent model of "on" diode of fig (a)
FIG (2.5 a, b, c)

$$V_D = V_T$$

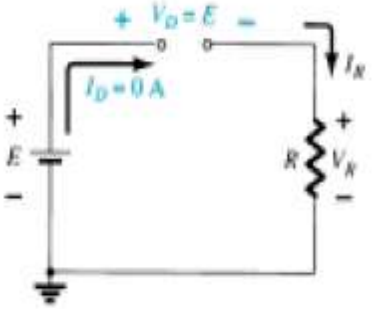
$$V_R = E - V_T$$

$$I_D = I_R = \frac{V_R}{R}$$





(a) Reversing diode of diode in fig(2.5 a) (b) determining the state of diode in fig(2.6 a)



(c) Substituting the equivalent model of 'off' diode of fig (2.6.a)

Fig (2.6 a, b, c)

The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.6. Due to the open circuit, the diode current is 0 A and the voltage across the resistor *R* is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = 0\text{ V}$$

Example 2.2: for series diode configurations of fig (2.7), determine VD.VR and ID.

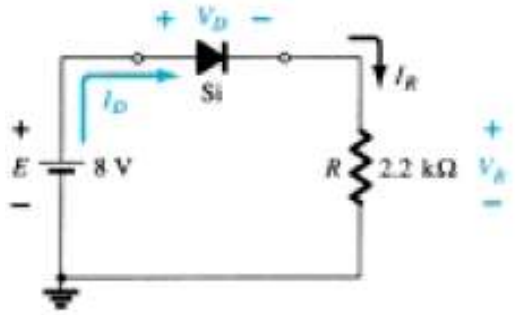


FIG (2.7)

Solution

Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\ V}$$

$$V_R = E - V_D = 8\ \text{V} - 0.7\ \text{V} = \mathbf{7.3\ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\ \text{V}}{2.2\ \text{k}\Omega} \cong \mathbf{3.32\ mA}$$

Example 3: for series diode configuration of fig (2.8), determine VD, VR and ID.

Solution:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})1.2\ \text{k}\Omega = \mathbf{0\ V}$$

And

$$V_D = E = \mathbf{0.5\ V}$$

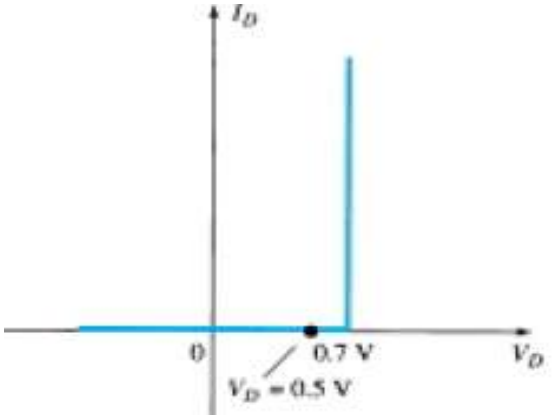
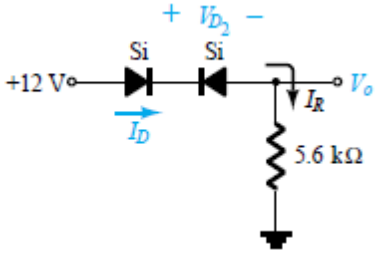
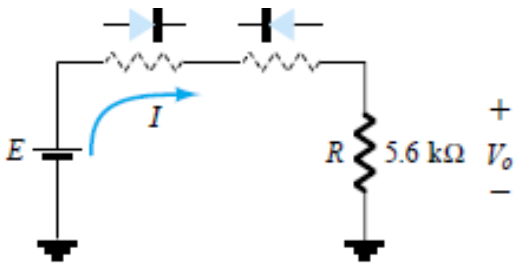


Fig (2.8)

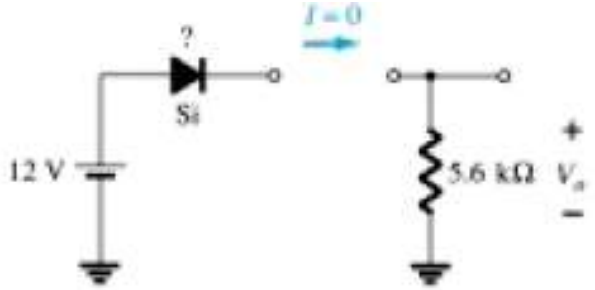
Example: determine ID.VD, V_o for circuit of fig (2.9)

Solution:

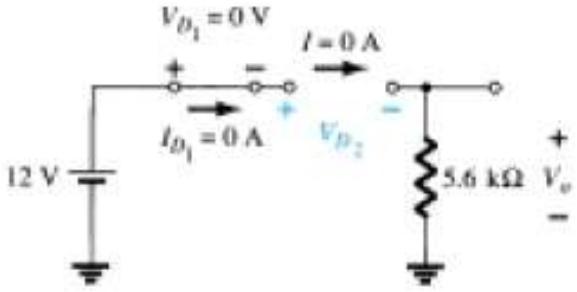




(a) Determine the state of diodes of circuit in the example



(b) Subsisting the equivalent state for the open diode



(c) Determine unknown quantities for circuit of example

$$V_o = I_R R = I_D R = (0\text{ A})R = 0\text{ V}$$

and
$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{12\text{ V}}$$

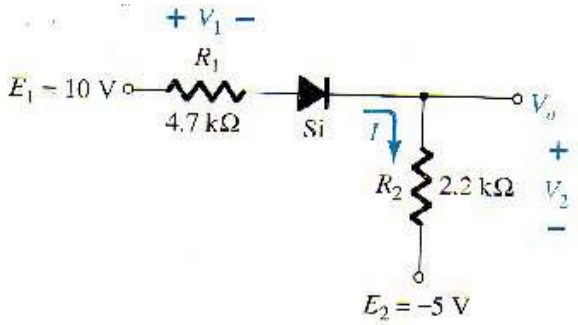
Applying Kirchhoff's voltage law in a clockwise direction gives us

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

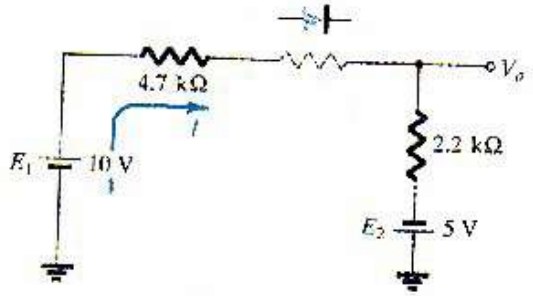
and
$$V_{D_2} = E - V_{D_1} - V_o = 12\text{ V} - 0 - 0$$
$$= \mathbf{12\text{ V}}$$

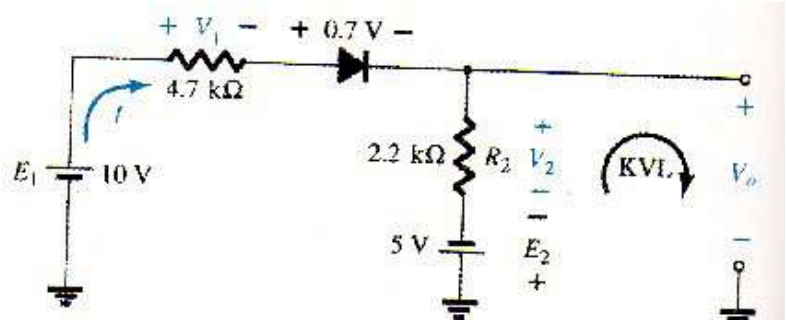
with
$$V_o = \mathbf{0\text{ V}}$$

Example 4: *Determine I, V_1, V_2 and V_O for the circuit of fig*



Solution:





$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$

$$\cong \mathbf{2.072\text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.072\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.74\text{ V}}$$

$$V_2 = IR_2 = (2.072\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.56\text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction will result in

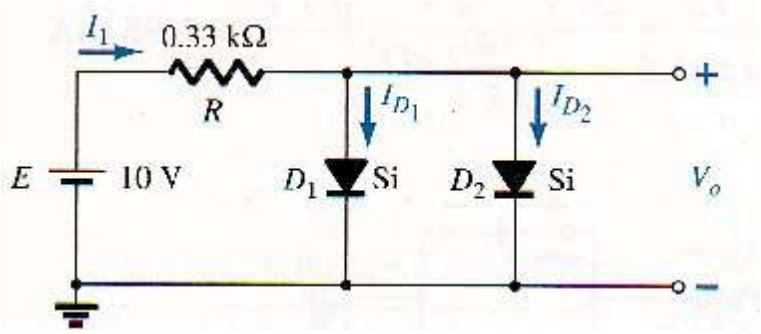
$$-E_2 + V_2 - V_o = 0$$

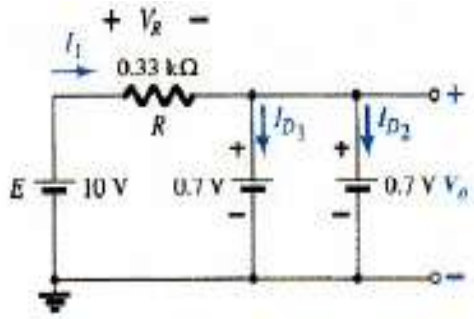
and

$$V_o = V_2 - E_2 = 4.56\text{ V} - 5\text{ V} = \mathbf{-0.44\text{ V}}$$

Parallel and series-parallel configurations:

Example 5: *Determine I_1, I_{D1}, I_{D2} and V_O for the circuit of fig:*





Solution:

$$V_o = \mathbf{0.7\ V}$$

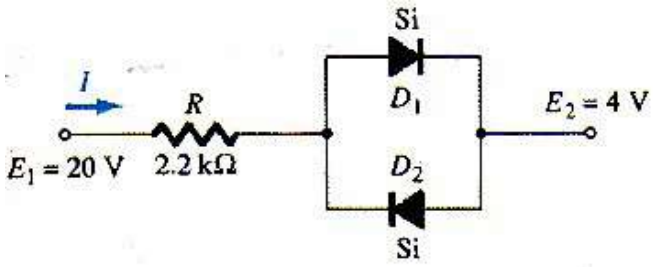
The current

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\ \text{V} - 0.7\ \text{V}}{0.33\ \text{k}\Omega} = \mathbf{28.18\ mA}$$

Assuming diodes of similar characteristics, we have

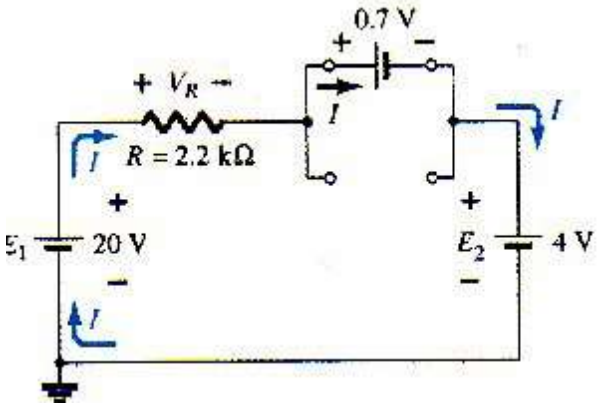
$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\ \text{mA}}{2} = \mathbf{14.09\ mA}$$

Example 6: *Determine the current I for the network of fig*



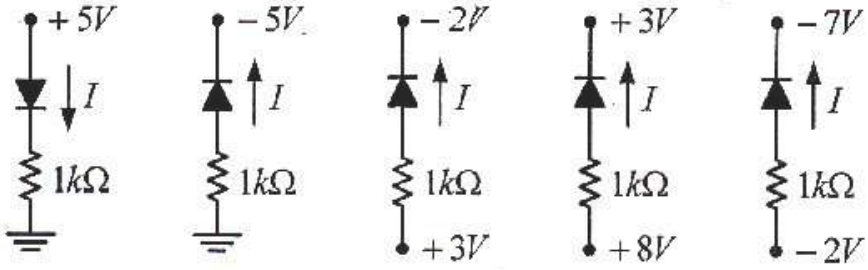
Solution:

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20\ \text{V} - 4\ \text{V} - 0.7\ \text{V}}{2.2\ \text{k}\Omega} \cong \mathbf{6.95\ mA}$$



Diode switching circuit

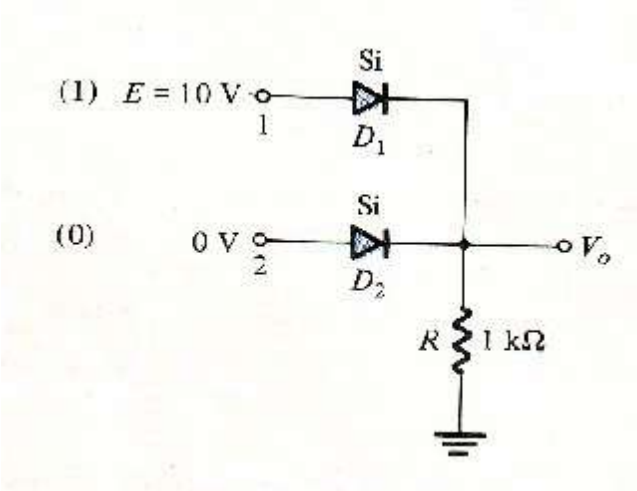
Diode switching circuits typically contain two or more diodes, each of which is connected to an independent voltage source. Understanding the operation of a diode switching circuit depends on determining which diodes, if any, are forward biased and which, if any, are reverse biased. The key to this determination ***is remembering that is a diode is forward biased only if its anode is positive with respect to it's cathode****.*



One of the very import applications of diode switching circuits is diode logic circuits ***AND/OR Gates.***

OR gate*: is such that the output voltage level will be a* ***1 if either or both input is a 1****. The 10V level is assigned a* ***1*** *for Boolean algebra while the 0V input is assigned a* ***0.***

Example 1: *Determine V_o for the network in fig:*



*D_1 is in the **on** state due to the applied voltage (10V) while D_2 is in the **off** state*

.

V_o = E - V_D = 10v - 0.7 = 9.3v

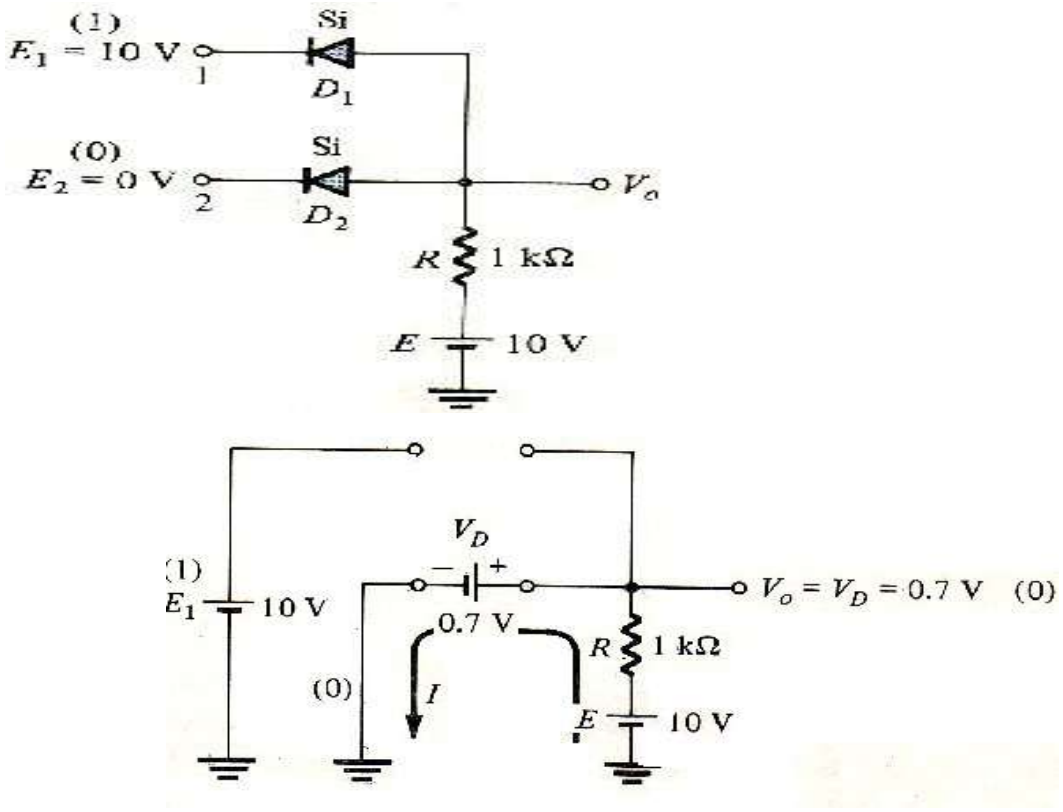
= (E - V_D) / R = (10-0.7) / 1KΩ = 9.3mA

*The output voltage level is not 10V as defined for an input of **1,** but the 9.3V is sufficiently at a **1** level with only one input.*

Input voltages		State of diodes		Output voltage
V_A	V_B	D_1	D_2	V_o
0	0	off	off	0
0	1	off	on	1
1	0	on	off	1
1	1	on	on	1

***AND gate**: is such that the output voltage level is will be **1 if both inputs are a 1**.*

Example 2: *Determine the output level for the positive logic **AND** gate of fig*:



*With 10v at the cathode D1 , is assumed that D1 is in the **off** state.*
*D2 is assumed to be in the **on** state due to the low voltage at the cathode side and the Availability of the 10v source through 1KΩ resistor. The voltage at Vo is 0.7v due to forward biased diode D2* ***i.e. I = (E-Vo) / R = (10-0.7) / 1KΩ = 9.3mA***

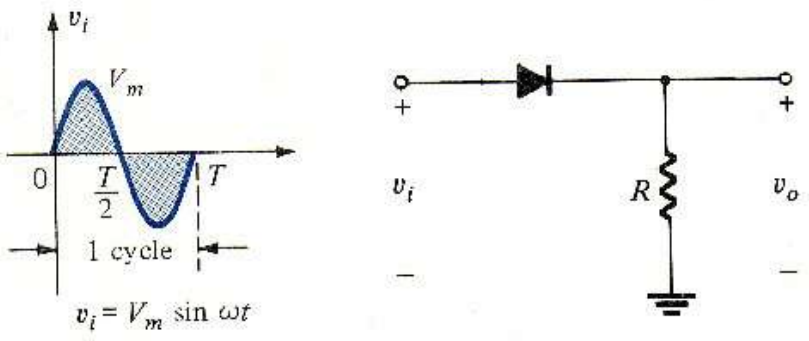
Input voltages		State of diodes		Output voltage
V_A	V_B	D_1	D_2	V_o
0	0	on	on	0
0	1	on	off	0
1	0	off	on	0
1	1	off	off	1

Lecture 10:

3. Half-Wave Rectifier:

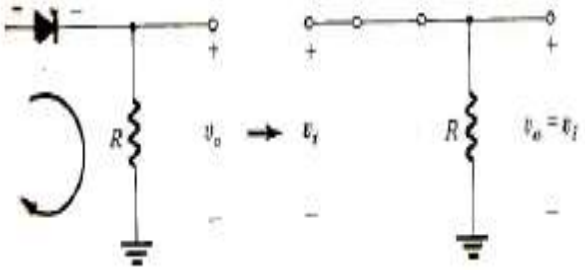
Half-wave rectification: is the process of ***removing one half of the input signal to establish a dc level****.*

The cct of the fig(3.1) called a half wave rectifiers will generates a waveform Vo that will have an average value of particular use in the ***ac– to–dc conversion process****.*



Fig(3.1) *half wave Rectifier*

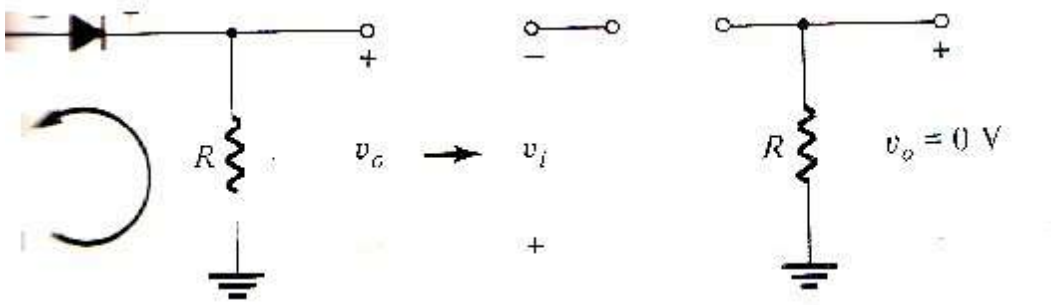
During the interval (t=0 to T/2) the polarity of the input voltage V_i is shown in fig(3.2)



Fig(3.3)conducting region(0 to T/2)

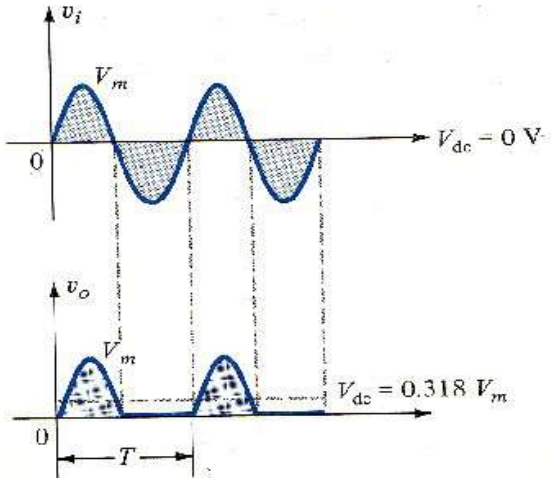
The result that for period 0 to T/2, Vo=Vi.

For period T/2 to T, the polarity of the input voltage Vi is shown in fig(3.4) and the ideal diode produces in off state, Vo=0V.



Fig(3.4) Non conducting region (T/2 to T)

An average value determined by average value determined by average dc value = $0.318V_m$



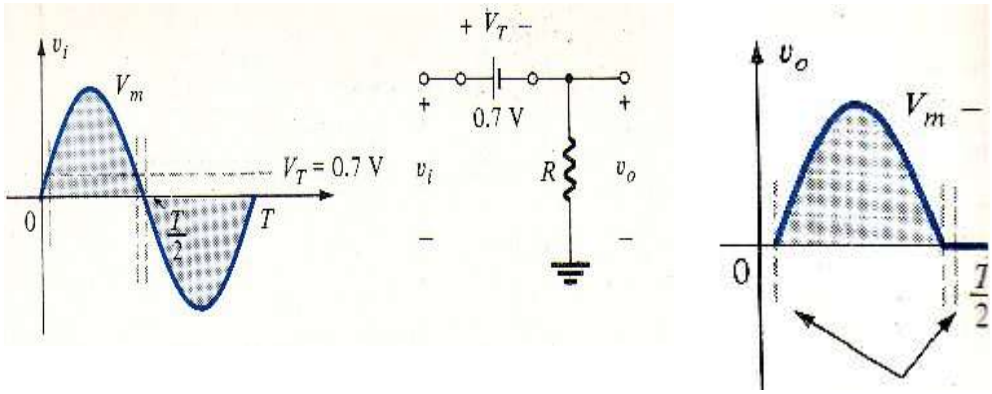
FIG(3.5) Half-Waves rectified signal

*The effect of using a silicon diode **with VT=0.7**V is shown by fig (2-20) for the forward bias. The input must now be at least 0.7V before the diode conducts.*

When conducting Vo =Vi - VT

If Vm > VT … i.e. Vdc= 0.318Vm

*if Vm is close to VT … i.e. Vdc ≈ 0.318(Vm – VT**)***

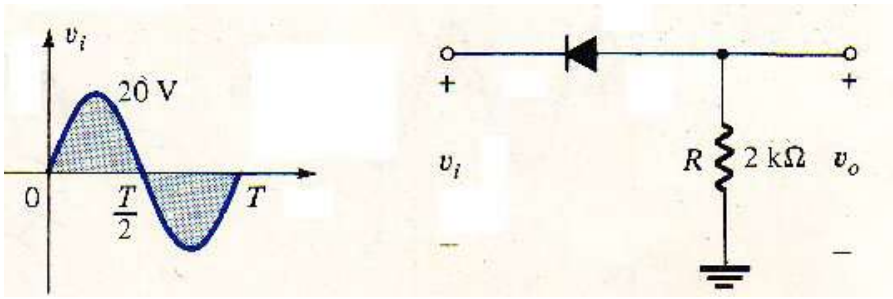


fig(3.6) Effect of VT on half-wave rectified signal

Example 1: for Half wave Rectifier:

(a) Sketch the output ***vo*** *and determine the dc level of the output for the network of Fig (3.7)*

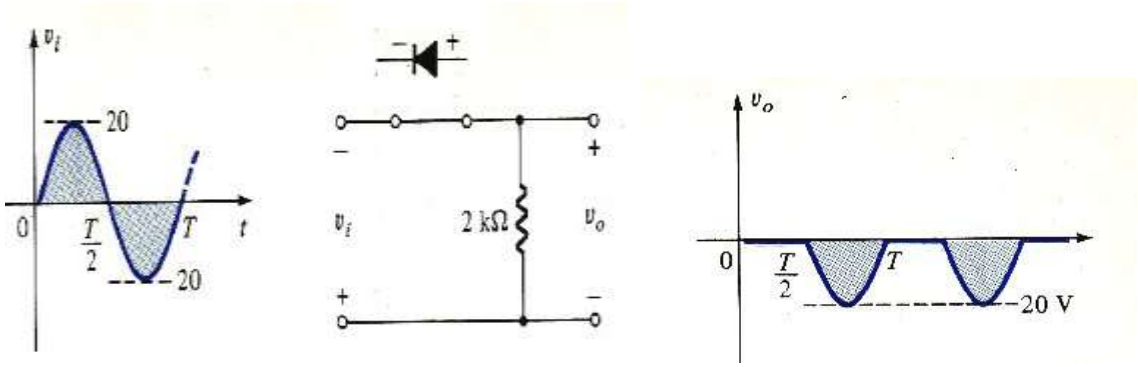
(b) Repeat part (a) if the ideal diode is replaced by ***a silicon*** *diode.*



Fig(3.7)

Solution:

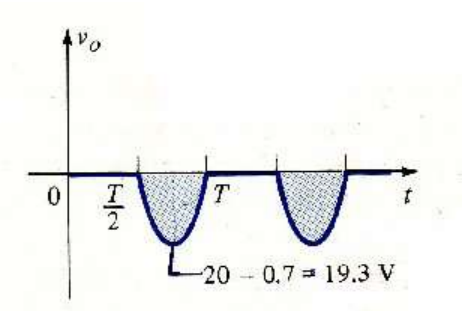
(a) In this situation the diode will conduct during the negative part of the input and ***vo*** *will appear as shown in fig (3.7)*



For full period, the DC level is:

$$V_{dc} = -0.318V_m = -0.318(20) = -6.36\ V$$

(b) Using a silicon diode, the output has the appearance of Fig (3.8)



4.Full-Wave Rectification

The dc level obtained from a sinusoidal input by half wave rectifier can be improved using a process called Full-Wave Rectification. Four diodes in a bridge configuration can be used as Full Wave Rectifier as shown in fig (4.1).

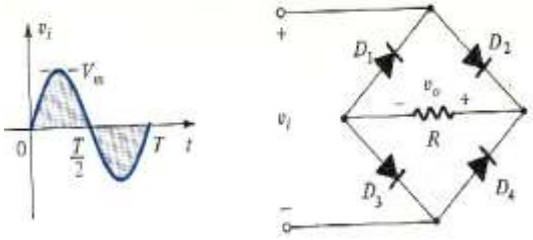


Fig (4.1) full –wave bridge rectifier

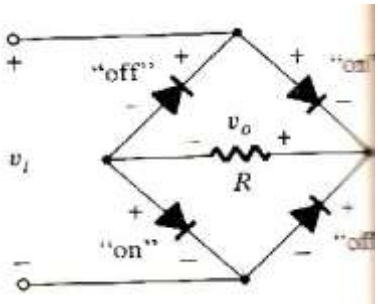


fig (4.2) network for period (0 to T/2)

*For the positive region of the input **the conducting** diodes are **D_2 & D_3** while **D_1& D_4** are in the **off state** as shown in fig (4.3).*

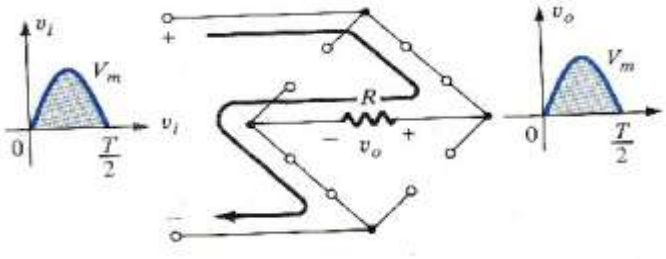
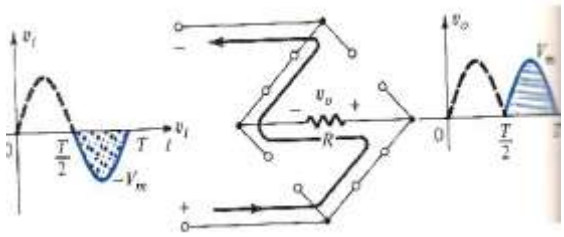


Fig (4.3)

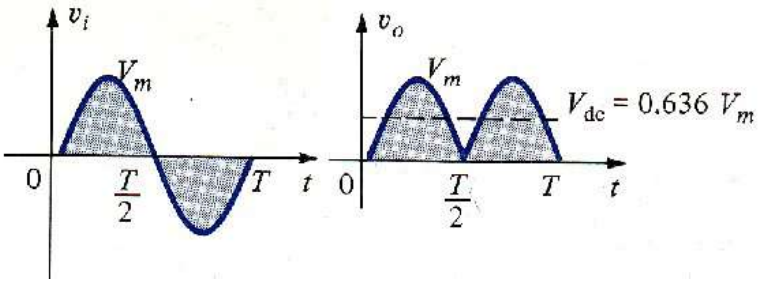
*For the negative region of the input **the conducting** diodes are **D_1 & D_4** while **D_2 & D_3** are in the **off state** as shown in fig (4.4)*



Fig(4.4)

The dc level for Full wave rectifier ***is twice that obtained for a half wave system***
i.e. average(d.c) level= 0.636V_m

Over one full cycle the input and output voltage is shown in fig (4.5)



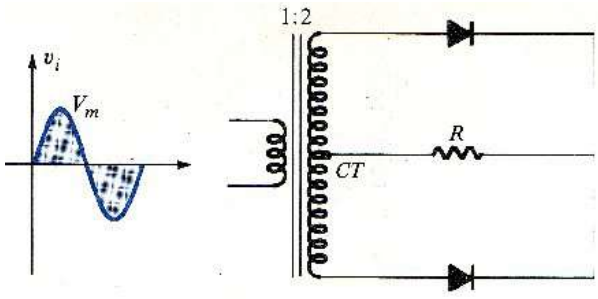
Fig(4.5)

The effect of Vo has also ***doubled****, as shown in fig (4.6) for silicon diodes during the Conduction state (for positive region).*

i.e. Vd.c=0.636Vm ***(Vm >> 2VT)***

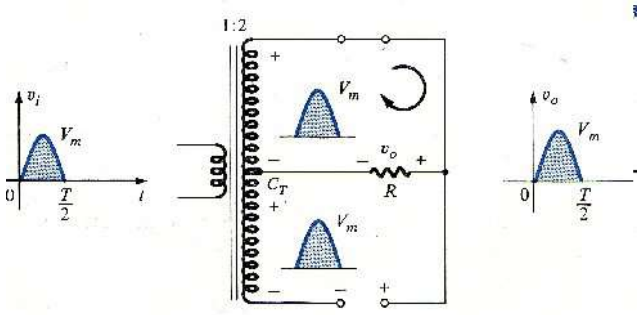
And if Vm is close to 2VT *i.e. Vd.c=0.636(Vm- 2VT)*

A second *popular full wave rectifier used only two diodes but requiring a* ***centre tapped (CT) transformer*** *to establish the input signal across each section of the secondary of the*
transformer as shown in fig (4.6).



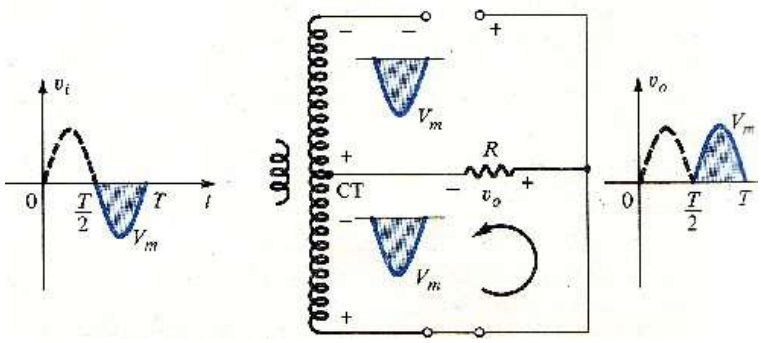
Fig(4.6)

*During the positive portion of V_i applied to the transformer, the diode **D_1** is **short circuit** and the diode **D_2** **is open circuit**.*



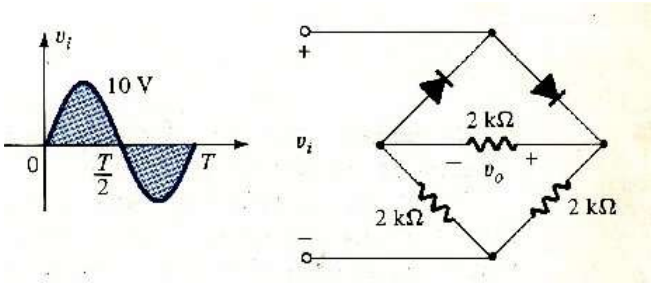
Fig(4.7)

*During the negative portion of V_i applied to the transformer, the diode **D_1** is **open circuit** and the diode **D_2** is **short circuit** as shown in fig (4.8).*



Fig(4.8)

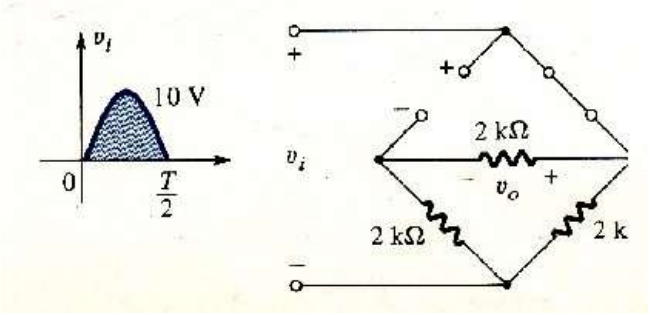
Example 2: for Full-wave rectifier.
Determine the output wave-form for the network of Fig (4.9) and calculate the output dc level



Fig(4.9)

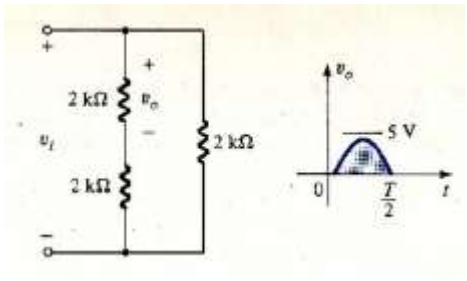
Solution:

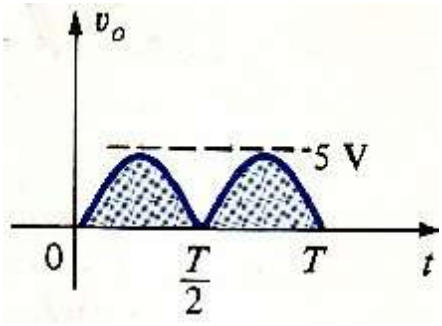
The network will appear as shown in Fig below for the positive region of the input voltage,



Where $v_o = 1/2 v_i$ ***or*** $V_{o(max)} = 1/2 V_{i(max)} = 1/2(10) = 5$ ***volt***

For the negative region of the input voltage the network will be appear as shown in Fig below:





The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5) = 3.18 \text{ volt}$$