Comparators

Chapter 10

Introduction

The second most widely used circuit block are comparators after OpAmps.

They are used extensively in A/D converters and other signal processing applications.

10.1.1 Input offset and noise

The input offset voltage of a comparator is the input voltage at which its output changes from one logic level to the other. It may be caused by device mismatch or may be inherent to the design of a comparator.

Random circuit noise can cause the output to change from one logic level to the other, even when the comparator input is held constant. Hence, in order to measure the input offset voltage in the presence of circuit noise, one would look for the input voltage that results in the output stage of the comparator being high and low with equal likelihood.

The input referred noise is then observed by changing the input around this value using output statistics assuming for example Gaussian distributions.

Example 10.1

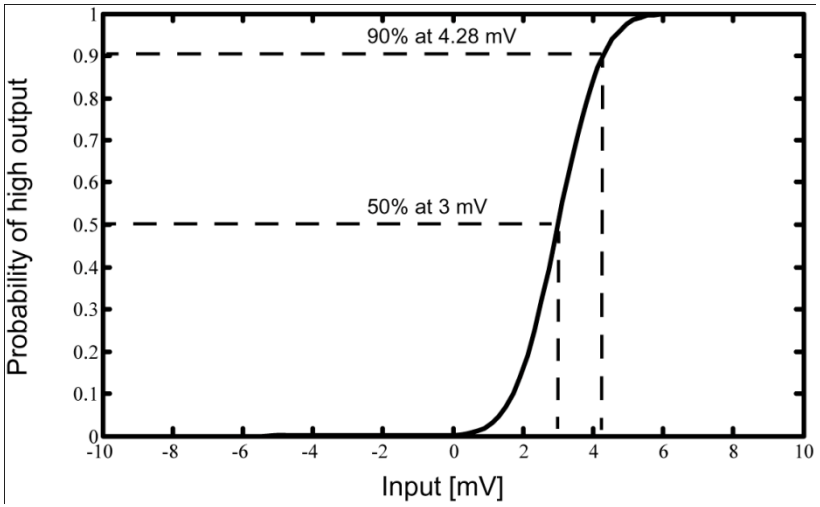
The output of a comparator is observed while slowly sweeping the input over the range −10 mV to +10 mV. The fraction of time that the comparator output is high is plotted as a function of the input voltage in Fig. 10.1. Estimate the comparator's input offset and noise. For this comparator, what is the smallest input that can be resolved with an error rate of 10^{-12}?

Solution

The plot in Fig. 10.1 is recognized as a normal distribution. At an input of 3 mV, the comparator output is equally likely to be high or low; hence, the comparator's input offset is 3 mV. The 90% confidence interval for a normal distribution is at 1.2816 times its standard deviation (rms) value. In Fig. 10.1, this occurs at an input of 4.28 mV, implying an rms input noise of

$$\frac{4.28 - 3}{1.2816}\ \text{mV} = 1\ \text{mV}_{\text{rms}}$$

For an error rate of 10^{-12}, the input must exceed the input offset by 7.0344 times the rms noise level. Hence, for a high output logic level the required input voltage is $3 + 7.0344 \cdot 1\ \text{mV} = 10.0\ \text{mV}$. For a low output logic level, the input must be below −4 mV.



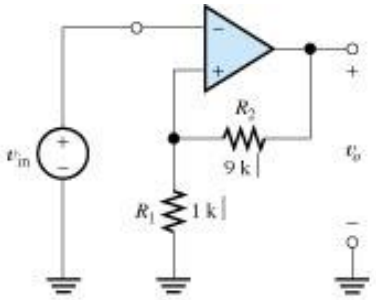
Chapter 10 Figure 01

10.1.2 Hysteresis

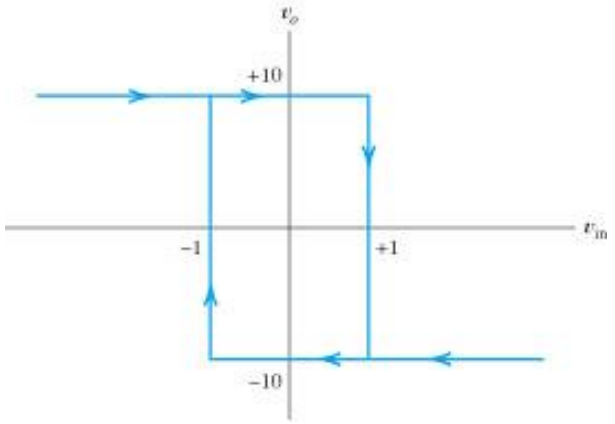
Many comparator designs have an input threshold that is dependent upon the past state of the comparator. Specifically, most comparators have a tendency to remain in their past state.

The comparator's "mem- ory" results from charge stored on the its internal capacitances, and is referred to as *hysteresis*. Generally, hysteresis is a nonideality in comparators that should be minimized, usually by ensuring all internal capacitances are completely discharged periodically. However, in some applications hysteresis may be used to advantage.

Recall the Schmitt Triggers discussed in E2 course.



(a) Circuit diagram of inverting Schmitt trigger

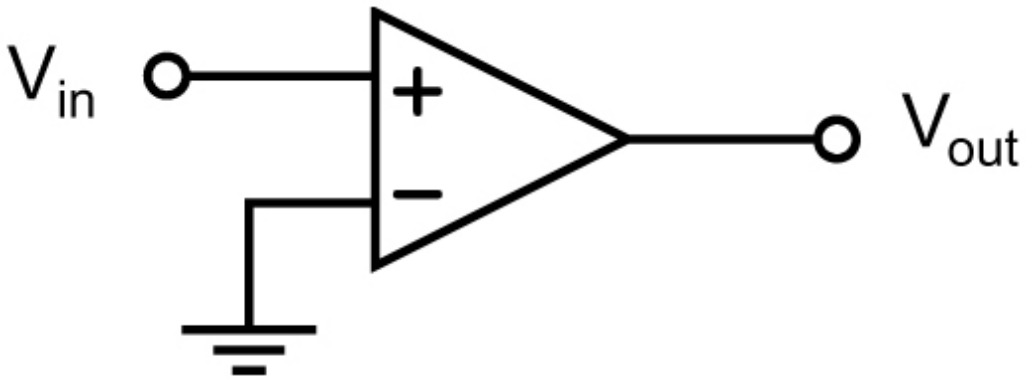


(b) Transfer characteristic displaying hysteresis

10.2 Using OpAmp as a comparator

A simple approach to realize a comparator is use an open-loop OpAmp. The main drawback of this approach is the slow response due to the slew rate of OpAmp.

Also, this approach has a resolution limited to the input offset voltage of the OpAmp, which might be in the order of 1 to 5mV for typical MOS process, and this may be inadequate for many applications.

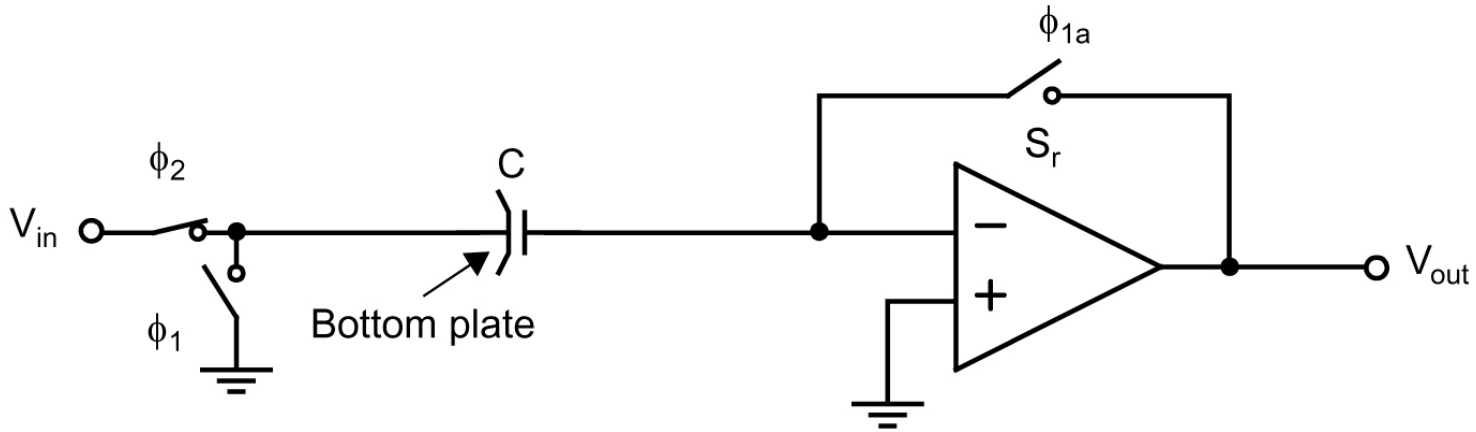


Chapter 10 Figure 02

An alternative design that can resolve signals with accuracies much less than the input offset voltage of OpAmps is to use switched capacitors with clocks.

The circuit of Fig. 10.3 operates as follows: During ϕ_1, known as the *reset phase,* the bottom plate[1] of the capacitor C (i.e., the left side of capacitor C) is connected to ground, and the top plate is connected to the inverting input of the opamp. At the same time, the output of the opamp is also connected to the inverting input of the opamp by closing switch S_r. Assuming the opamp is ideal, this connection causes the capacitor to be charged to zero volts. Next, during the *comparison phase*, the reset switch, S_r, is turned off, and the bottom plate of the capacitor is connected to the input voltage. The opamp is now in an open-loop configuration. If the input signal is greater than zero, the output of the opamp swings to a large negative voltage. If the input signal is less than zero, the output of the opamp swings to a large positive voltage. These two cases are easily resolved and the decision can be stored using a simple digital latch.

The limitations of this approach become apparent when one considers nonideal opamps, which have finite gains and require compensation to be stable during the reset phase.



Chapter 10 Figure 03

Clock ϕ_{1a} is a slightly advanced version of ϕ_1

Example 10.2

Consider the case in which a 0.2-mV signal must be resolved using the circuit shown in Fig. 10.3, where the opamp's output should be 2 V. Assuming the opamp's unity-gain frequency is 10 MHz, find the maximum clocking rate of the comparator circuit if reset and comparison phases are equal and if six time constants are allowed for settling.

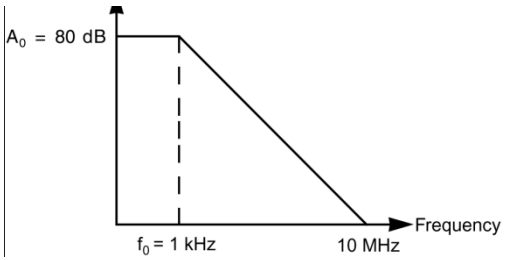
After the comparison phase, the output of the opamp should have a 2-V difference between the cases in which the input signal is either –0.1 mV or +0.1 mV.[2] As a result, the opamp gain must be at least 10,000 V/V. By assuming that the dominant-pole compensation is used to guarantee stability during the reset phase, we obtain an open-loop transfer function for the opamp similar to that shown in Fig. 10.4. Here, the –3-dB frequency of the opamp is given by

$$f_{-3\ dB} = \frac{f_t}{A_0} = 1\ kHz \tag{10.1}$$

During the comparison phase, the output of the opamp will have a transient response similar to that of a first-order system that has a time constant given by

$$\tau = \frac{1}{2\pi f_{-3\ dB}} \cong 0.16\ ms \tag{10.2}$$

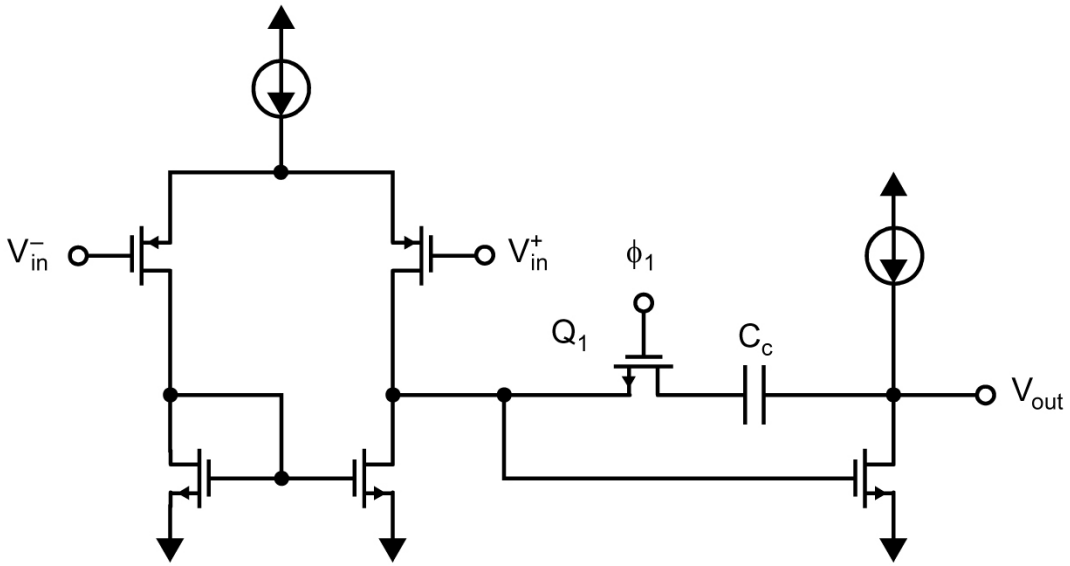
If six time constants are allowed for settling during the comparison phase, then approximately 1 ms is needed for the comparison phase. Assuming the reset time is the same as the comparison time, the clock frequency can be no greater than 500 Hz—a frequency that is much too slow for most applications.



Chapter 10 Figure 04

One possible way to speed up the comparison is to disconnect the compensation capacitor during the comparison phase. (in the circuit shown below, Q1 is used to achieve lead compensation). This improves the speed to tens of kHz range, still slow for some applications.

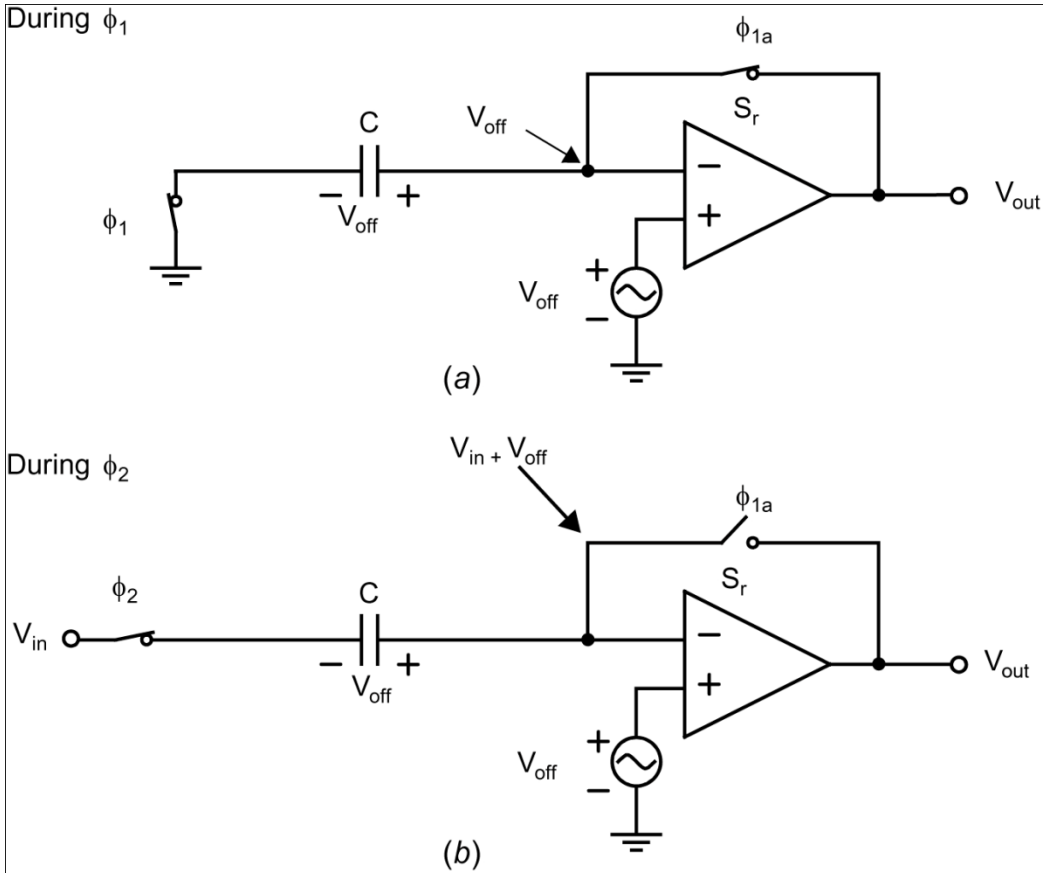
One superior aspect of the previous circuit is that the input capacitor C is never charged or discharged during operation. This approach minimizes the charge required from the input when V_{in} changes.



Chapter 10 Figure 05

10.2.1 input offset voltage errors

In switched-capacitor comparators, such as that shown in Fig. 10.3, input offset is not a problem since it is stored across the capacitor during the reset phase, and then the error is cancelled during the comparison phase.



Chapter 10 Figure 06

This techniques also remove low frequency 1/f noise, which can be large in CMOS circuits.

10.3 Charge injection errors

Perhaps the major limitation on the resolution of comparators is due to charge injection, also called clock feed-through. This error is due to unwanted charges being injected into the circuit when the transistor turns off.

Suppose the switches are realized by nMOS transistors. When they are on, they operate in triode region and have zero drain-source voltages. When they turn off, charge errors occur by two mechanisms.

This first one is due to channel charge, which must flow out from the channel region of the transistor to drain and source junctions. The channel charge of a transistor with zero V_{ds} voltage is

$$Q_{ch} = WLC_{ox}V_{eff} = WLC_{ox}(V_{GS} - V_t) \tag{10.3}$$

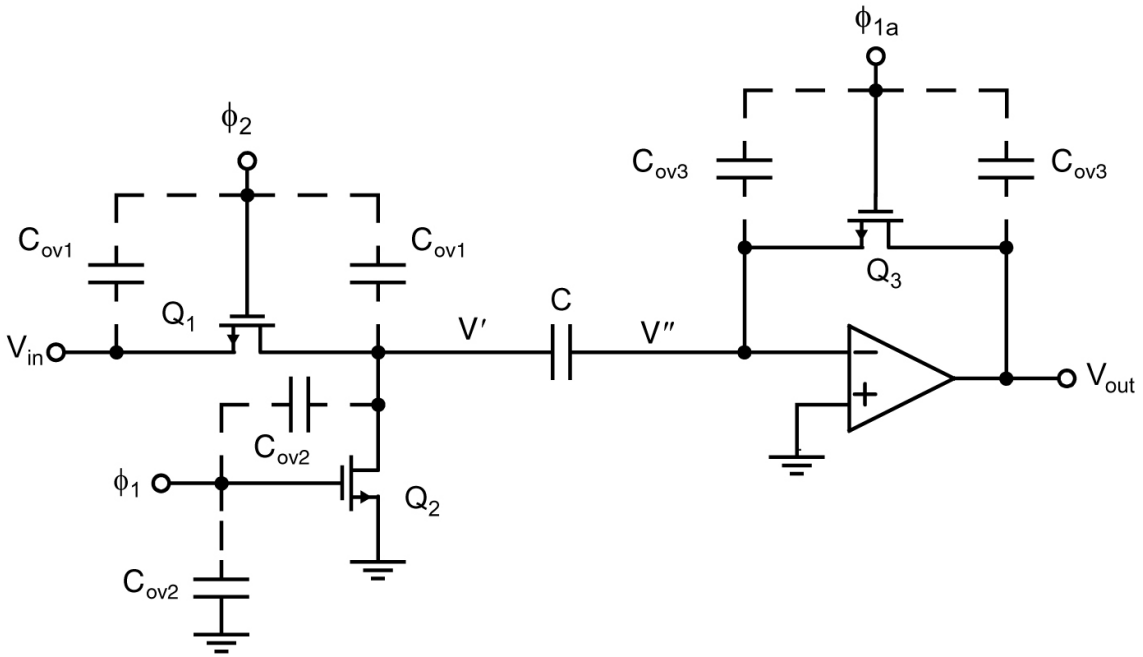
This charge often dominates. The second charge (typically smaller, unless V_{eff} is very small) is due to the overlap capacitance between the gate and the junctions.

10.3 Charge injection errors

Consider first when Q_3 turns off. If the clock waveform is very fast, the channel charge due to Q_3 will flow equally out through both junctions [Shieh, 1987]. The $Q_{ch}/2$ charge that goes to the output node of the opamp will have very little effect other than causing a temporary glitch. However, the $Q_{ch}/2$ charge that goes to the inverting-input node of the opamp will cause the voltage across C to change, which introduces an error. Since this charge is negative, for an n-channel transistor, the node voltage V'' will become negative. The voltage change due to the channel charge is given by

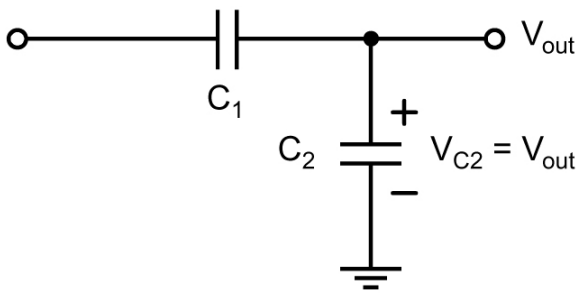
$$\Delta V'' = \frac{(Q_{ch}/2)}{C} = -\frac{V_{eff3}C_{ox}W_3L_3}{2C} = -\frac{(V_{DD}-V_{tn})C_{ox}W_3L_3}{2C} \tag{10.4}$$

since the effective gate-source voltage of Q_3 is given by $V_{eff3} = V_{GS3} - V_{tn} = V_{DD} - V_{tn}$. The preceding voltage change in V'' is based on the assumption that Q_2 turns off slightly after Q_3 turns off.



Chapter 10 Figure 07

To calculate the change in voltage due to the overlap capacitance, it is first necessary to introduce the capacitor-divider formula. This formula is used to calculate the voltage change at the internal node of two series capacitors, when the voltage at one of the end terminals changes. This situation is shown in Fig. 10.8, where it is assumed that V_{in} is changing and we want to calculate the change in $V_{out} = V_{C2}$. The series combination of C_1 and C_2 is equal to a single capacitor, C_{eq}, given by



Chapter 10 Figure 08

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{10.5}$$

When V_{in} changes, the charge flow into this equivalent capacitor is given by

$$\Delta Q_{eq} = \Delta V_{in} C_{eq} = \Delta V_{in} \frac{C_1 C_2}{C_1 + C_2} \tag{10.6}$$

All of the charge that flows into C_{eq} is equal to the charge flow into C_1, which is also equal to the charge flow into C_2. Thus, we have

$$\Delta V_{out} = \Delta V_{C2} = \frac{\Delta Q_{C2}}{C_2} = \frac{\Delta V_{in} C_1}{C_1 + C_2} \tag{10.7}$$

This formula ca be applied to the previous circuit. Assuming clock signal changes from V_{dd} to V_{ss}, the change in V'' due to overlap capacitance is

$$\Delta V'' = \frac{-(V_{DD} - V_{SS}) C_{ov}}{C_{ov} + C} \tag{10.8}$$

This change is normally less than that due to the change caused by the channel charge since C_{ov} is small.

Example 10.3

Assume that a resolution of ±2.5 mV is required from the circuit of Fig. 10.7. The following values are given: $C = 0.1$ pF, $C_{ox} = 8.5$ fF/(μm)^2, $(W/L)_3 = 4$ μm/0.2 μm, $L_{ov} = 0.04$ μm, $V_{tn} = 0.45$ V, and $V_{DD} = 1$V. What is the change in $\Delta V''$ when Q_3 turns off?

Solution

Using (10.4), we have $\Delta V'' = -53$ mV. The overlap capacitance is given by $C_{ov} = W_3 L_{ov} C_{ox} = 1.4$ fF. Using (10.8), this gives a voltage change in $\Delta V''$ of $\Delta V'' = -2.8$ mV, which is smaller than the change due to the channel charge, but not insignificant. The total change is found by adding the two effects so that $\Delta V'' = -56$ mV.

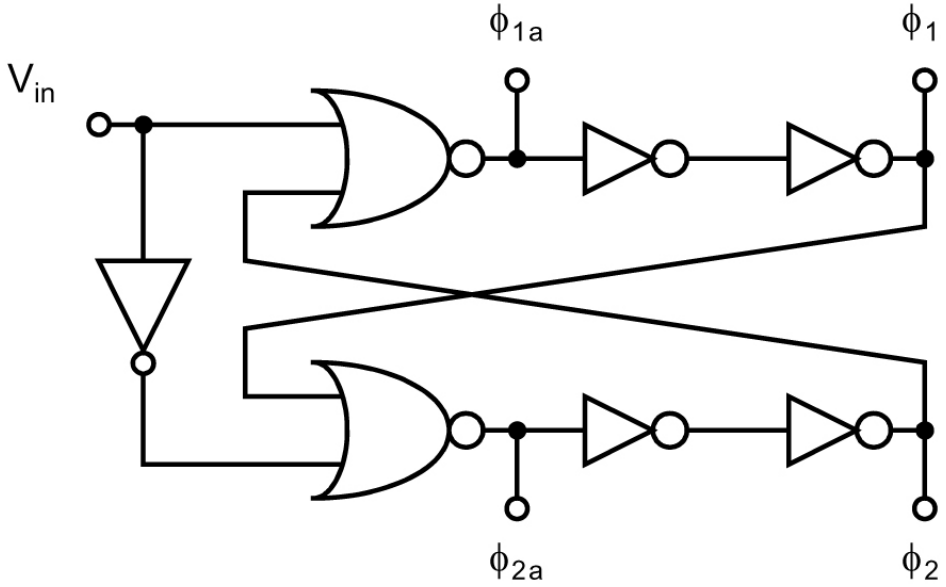
This result is on the order of 10 times greater than the value of ±2.5 mV that should be resolved. Clearly, additional measures should be taken to minimize the effects of charge-injection if this resolution is required.

10.3.1 Making charge injection signal indepedent

Charge injection due to Q1/2 may cause temporary glitches, but have much less effect than Q3 if Q2 turns off slightly after Q3. This is why the clock of Q3 is in advance of Q2.

When Q2 turns off, its charge injection causes a negative glitch at V', but not any change in the charge stored on C since right hand side of C is open circuit.

Later, when Q1 turns on, the voltage V' will settle to V_{in} regardless of the charge from Q2 and the voltage across C is unaffected. The charge injection of Q1 has no effect either as again the right hand side of C is connected to an open circuit.



Chapter 10 Figure 09

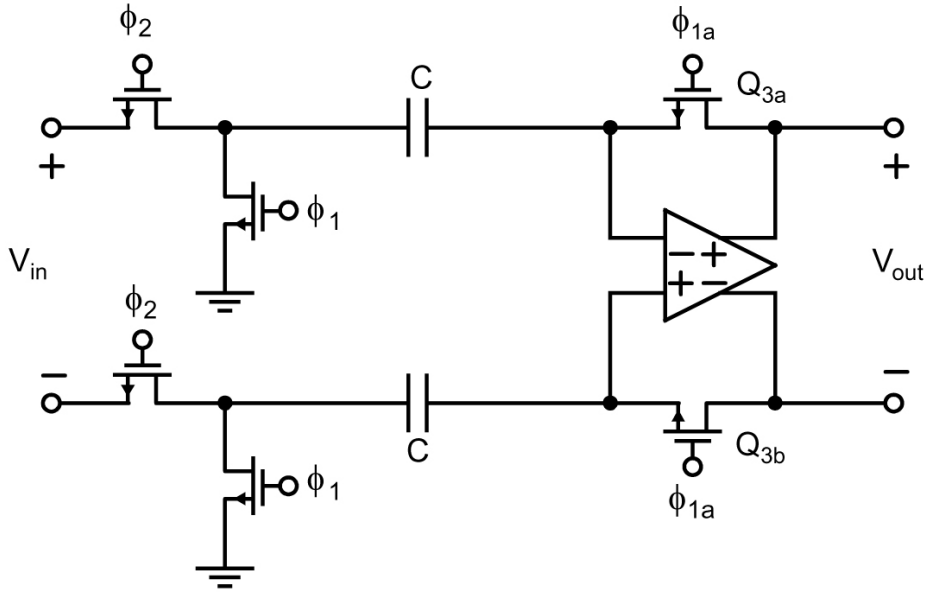
Non-overlapping clocks are needed. One circuit is shown here.

10.3.2 Minimizing charge injection errors

The simplest way to reduce errors due to charge-injection is to use larger capacitors. For our previous example, capacitors on the order of about 10 pF guarantee that the clock-feedthrough errors are approximately 0.5 mV. Unfortunately, this large amount of capacitance would require a large amount of silicon area.

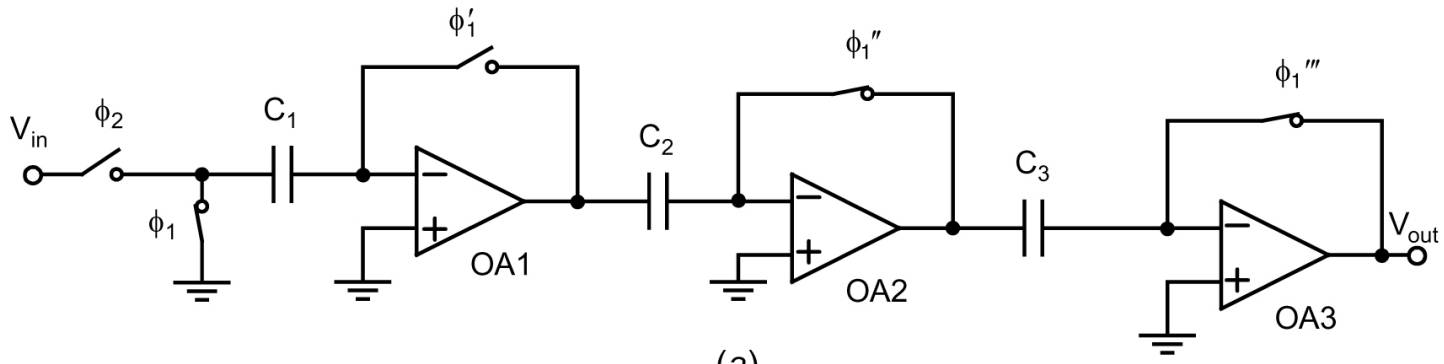
An alternative approach for minimizing errors due to charge-injection is to use fully differential design techniques for comparators, similar to what is often done for opamps. A simple example of a one-stage, switched-capacitor, fully differential comparator is shown in Fig. 10.10.

Ideally, when the comparator is taken out of reset mode, the clock feedthrough of reset switch Q_{3a} matches the clock feedthrough of Q_{3b}. The only errors now are due to mismatches in the clock feedthrough of the two switches, which will typically be at least ten times smaller than in the single-ended case.



Chapter 10 Figure 10

A third alternative that can be used along with fully differential design techniques is to realize a multi-stage comparator [Poujois, 1978; Vittoz, 1985], where the clock feedthrough of the first stage is stored on coupling capacitors between the first and second stage, thereby eliminating its effect. The clock feedthrough of the second stage can be stored on the coupling capacitors between the second and the third stages, and so on.



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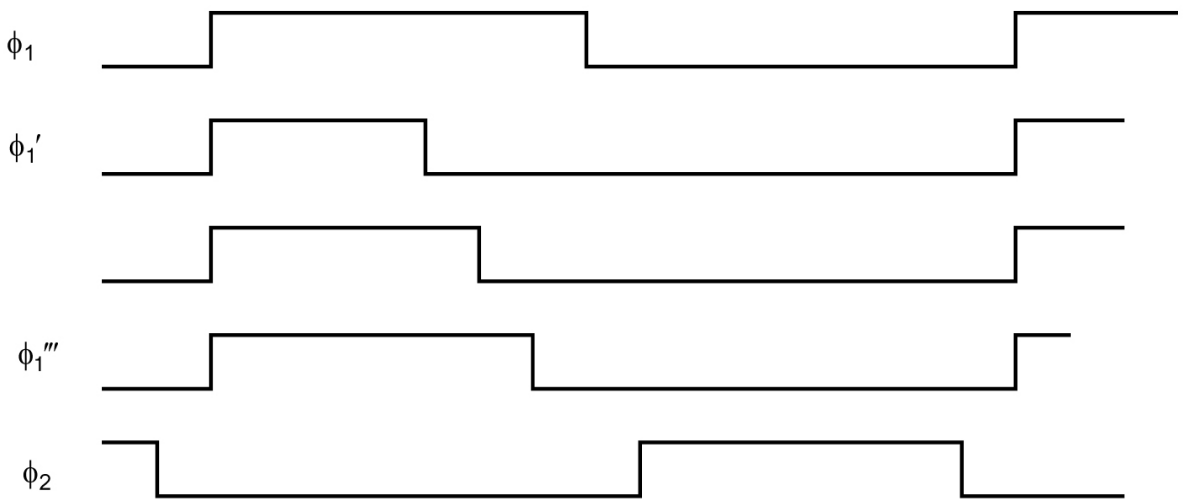
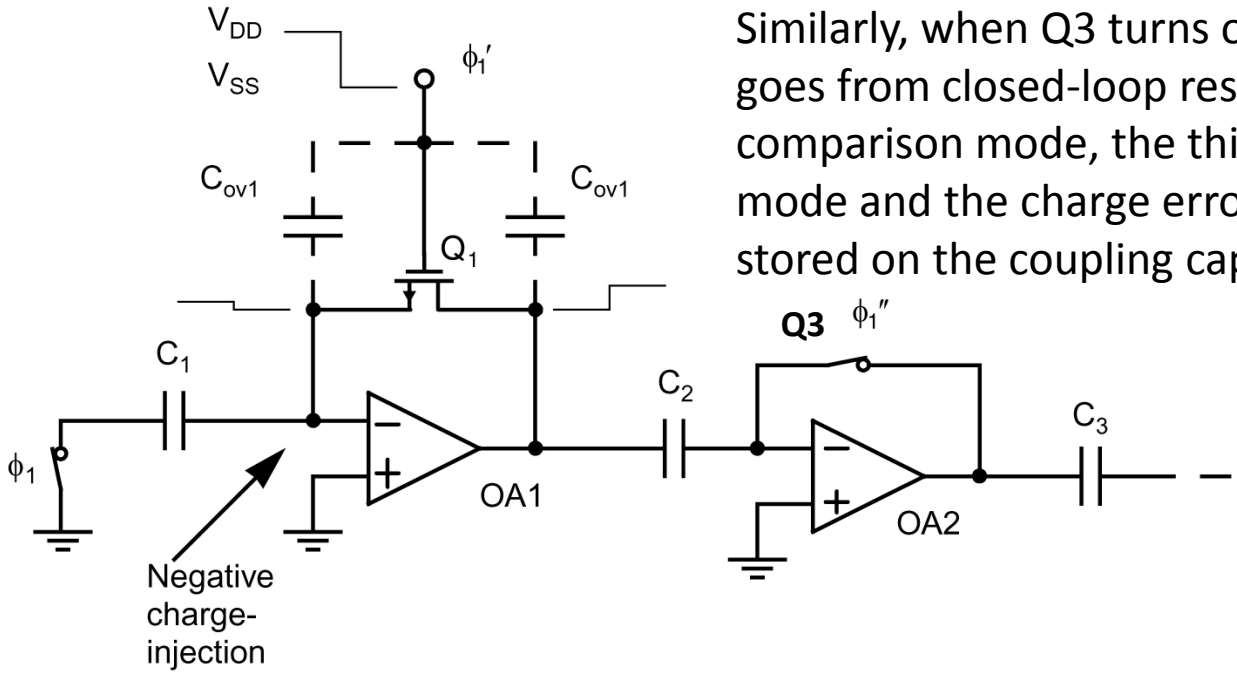


(*b*)

Chapter 10 Figure 11

Consider the time that Q1 turns off and introduces charge injection error, as shown below in the equivalent circuit. Q injects charge into both the inverting input and output of the first stage through overlap capacitors. For the OA1 output, it causes only a a temporary glitch (as C2 is connected to GND). The OA1 inverting terminal becomes negative by the amount calculated using the method before.

After the OA1 inverting terminal become negative, the OA1 output becomes positive by an amount equal to gain of OA1 multiplied by the negative change. However, at this time Q3 is still on, so the second stage is still being rest and C2 is charged up to the output error caused by the injection error of the first stage, thereby eliminating its effect.



Similarly, when Q3 turns off and the second stage goes from closed-loop reset mode to open-loop comparison mode, the third stage is still in reset mode and the charge error of the second stage is stored on the coupling capacitor C3.

Finally, when the third stage turns off, its charge error is not cancelled, but the error it causes in resolving an input voltage to all three stages is small (divided by the gain when referred to the input).

Chapter 10 Figure 12

Example 10.4

Assume all capacitors are 0.1 pF, transistor sizes are $W/L = 4\ \mu m/0.2\ \mu m$, $C_{ox} = 8.5\ fF/(\mu m)^2$, $L_{ov} = 0.04\ \mu m$, $V_{tn} = 0.45V$, and $V_{DD} = 2\ V$, and each stage has a gain of 20. What is the input-offset voltage error caused by the clock feedthrough of the third stage when the third stage comes out of reset?

Solution

The values used are identical to those used in Example 10.3. Therefore, the charge-injection at the inverting input of the third stage is the same as that found in the solution to Example 10.3, or −56 mV. The input signal that can overcome this value 56 mV is given by

$$\Delta V_{in} = \frac{56\ mV}{A_1 A_2} = 140\ \mu V \tag{10.9}$$

Thus, the equivalent input-offset voltage is 140 μV, which is much better than the resolution found in Example 10.3 of 56 mV.

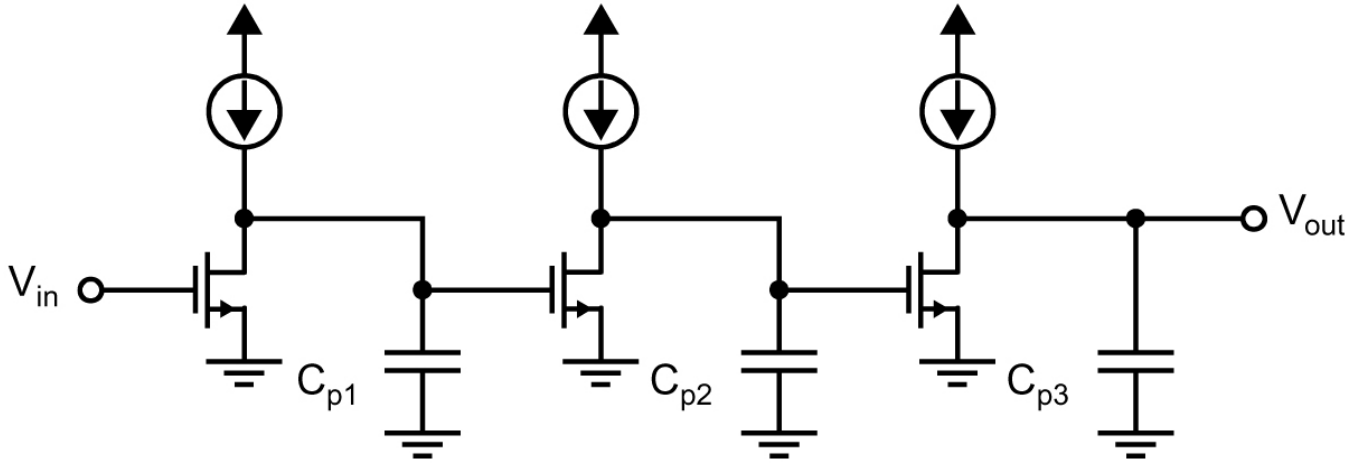
10.3.3 Speed of multi-stage amplifiers

Although the multi-stage approach is limited in speed due to the need for the signal to propagate through all the stages, it can still be reasonably fast because each of the individual stages can be made to operate fast. Typically, each stage consists of a single-stage amplifier that has only a $90°$ phase shift and therefore does not need compensation capacitors (i.e., each stage has a $90°$ phase margin without compensation).

The circuit below shows a cascade of first-order uncompensated Common-source amplifiers. It can be estimated that the time constant of the cascade stage is approximately equal to 3 times the time constant of a single stage, usually must faster than an OpAmp.

$$\tau_{total} \cong \frac{2nA_0C_{gs}}{g_m} \cong \frac{4nA_0L^2}{3\mu_n V_{eff}}$$

So, to design high speed comparators, one should make V_{eff} of each stage large. However, this tradeoff with W/L, which should be relatively large given a fixed current in order to have large g_m so that input referred noise is small.



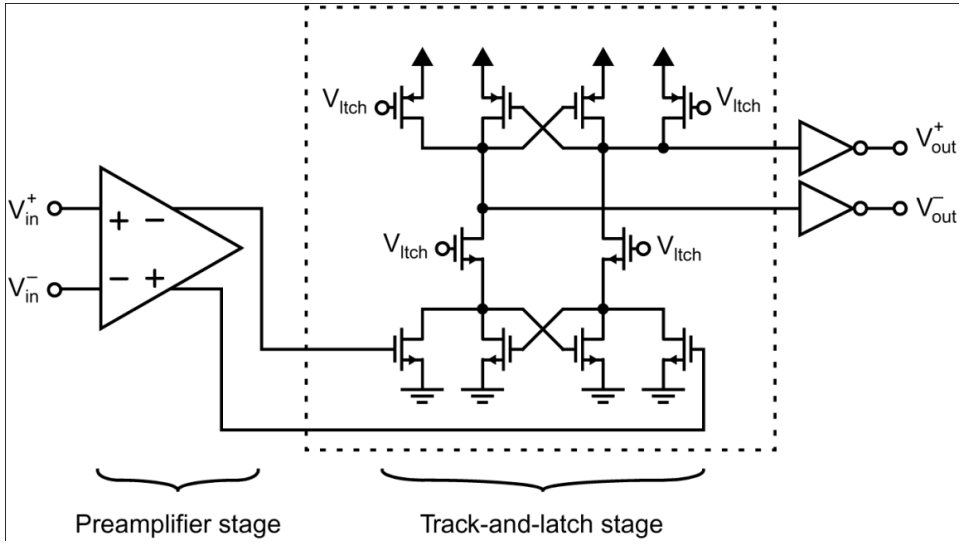
Chapter 10 Figure 13

10.4 Modern track-and-latch comparators

Modern high-speed comparators typically have one or two stages of pre-amplification followed by a track-and-latch stage, as the one shown below.

The rationale : the preamplifier is used to obtain higher resolution and to minimize the effects of kickback (explained later). The output of preamplifier, though larger than the comparator input, is typically still much smaller than needed to drive digital circuits. So then the track-and-latch stage further amplifiers this signal during the track phase and then amplifies it again during the latch phase.

Positive feedback is usually used in the latch phase to amplify the signal to full-scale digital output. The track-latch stage minimizes the number of gain stages needed, thus improve the feedback compared to the multiple stage approach discussed before.

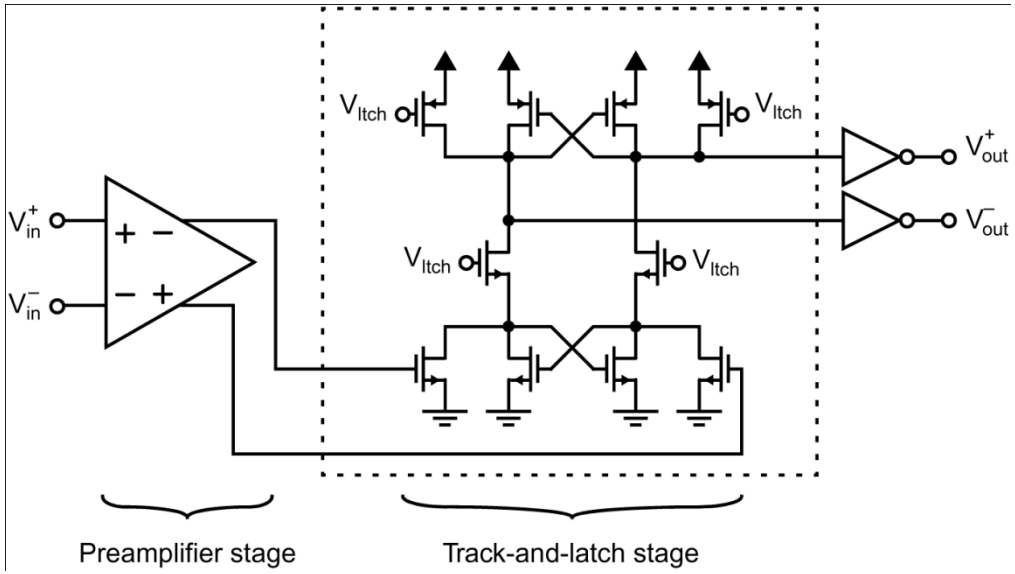


Chapter 10 Figure 14

The pre-amplifier typically has some gain, say between 2 to 10, but not larger than 10 as otherwise its time constant may be too large so as to limit its speed. One or two simple resistively-loaded differential amplifiers are often suitbale.

Note also that the input offset and noise of the track-and-latch stage are attenuated by the gain of the pre-amp when referred to the input, so the pre-amp's noise and offset mostly dominates.

It is not good practice to eliminate the pre-amp since kickback into the driving circuitry will then result in very limited accuracy. Kickback denotes the charge transfer either into or out of the inputs when the track-and-latch stage goes from track mode to latch mode.



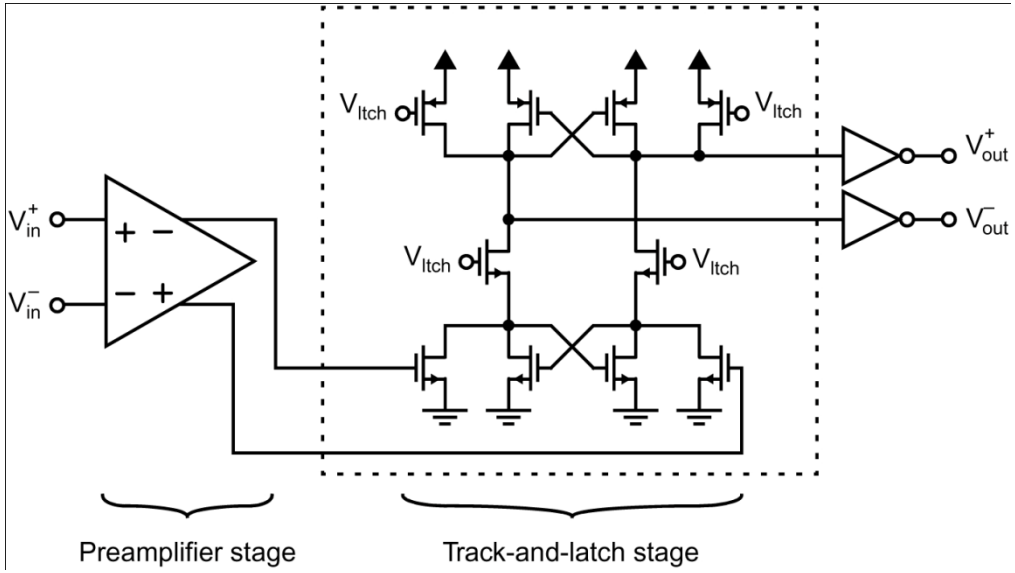
Chapter 10 Figure 14

This charge transfer is caused by the charge needed to turn the transistors in the positive feedback circuit on and by the charge that must be removed to turn transistors in the tracking circuit off. Without a pre-amp, this kickback will enter the driving circuitry and cause very large glitches.

In high-resolution applications, capacitive couplings and reset switches are also included to eliminate any input-offset voltage and clock feedthrough errors, similar to what is discussed before.

One very important consideration for comparators is to ensure that no memory is transferred from one decision cycle to the next, so as to cause hysteresis.

To minimize hysteresis, one can reset the different stages before entering tracking mode for next cycle. This may be achieved by connecting internal nodes to power supplies or by connecting differential nodes together using switches before entering track mode. (see the circuit below using V_{itch} signal to reset nodes to VDD and GND). This actually helps speed up the operation for next cycle's comparison, especially for small amplitude signals.



Chapter 10 Figure 14

Gain in track mode should not be too large either, as this may limit the speed.

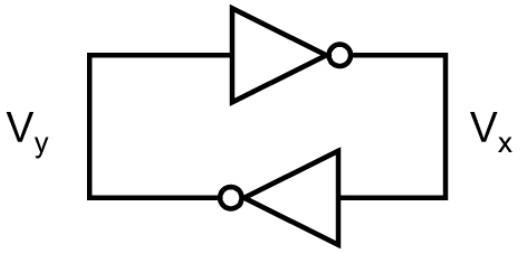
10.4.1 Latch-mode time constant

The time constant of the latch when in positive feedback may be found by analyzing a simplified circuit consisting of two back-to-back inverters.

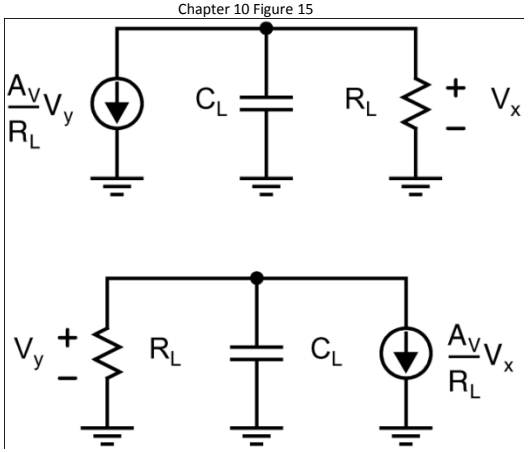
If we assume that the output voltages of the inverters are close to each other at the beginning of the latch phase and that the inverters are in their linear range, then each inverter can be modelled by a voltage-controlled current source driving an RC load.

It can be estimated that to reach ΔV_{logic} with an initial ΔV_0, it takes (see page 428 for detail)

$$T_{ltch} = \frac{C_L}{G_m} \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) = K_3 \frac{L^2}{\mu_n V_{eff}} \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right)$$



Chapter 10 Figure 15



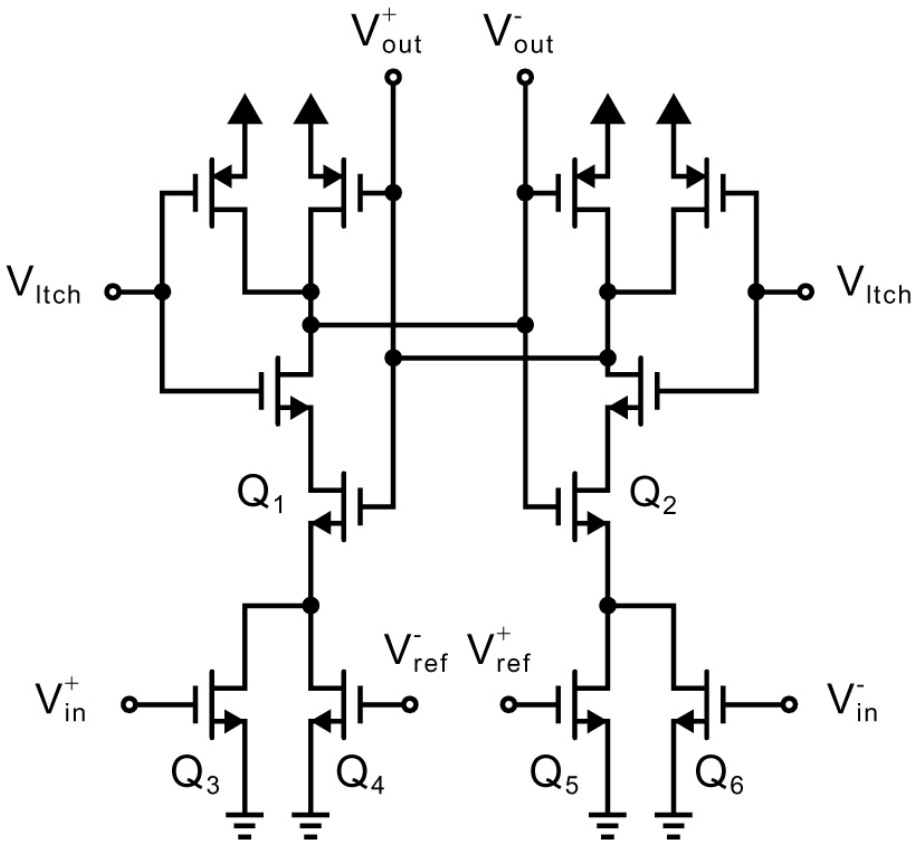
Chapter 10 Figure 16

So, we want small length for inverter, relatively large V_{eff} for fast operation.

When, ΔV_0 is too small, an issue called meta-stability may occur as it takes too long to get to the desired logic level ΔV_{logic}.

10.4.2 Latch offset

The input offset of a latch is influenced by random and systematic mismatch between its two half-circuits. When very small transistors are used, this mismatch may be significant often leading of offset of 10's of mV or more. In such cases, additional components may be introduced to so that by appropriately controlling the imbalances in the circuit, the effects of random mismatch can be cancelled, resulting in a latch with near-zero overall offset.



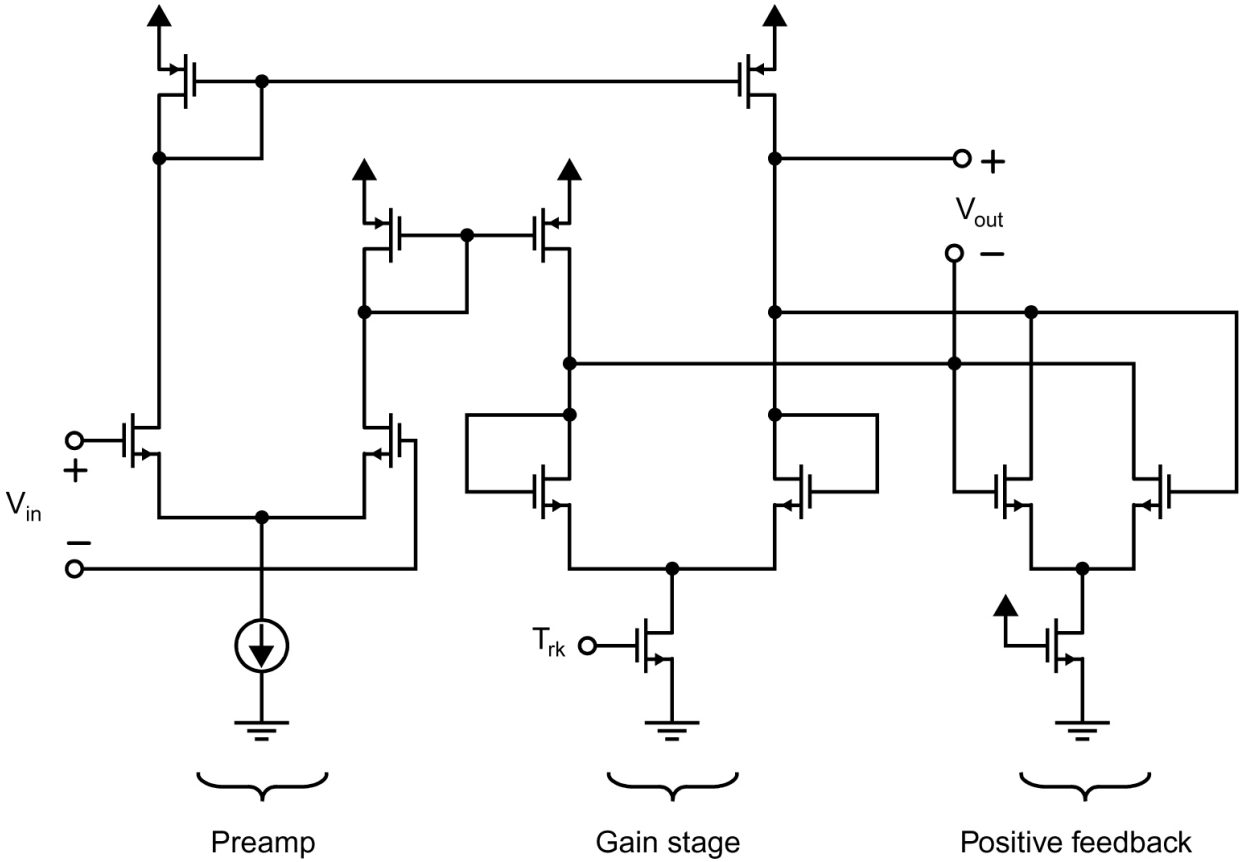
Chapter 10 Figure 19

The example circuit uses additional V_{ref} voltages to counteract the inbalance of the latch.

10.5 Some examples of comparators

This one below has the positive feedback of the second stage always enabled.

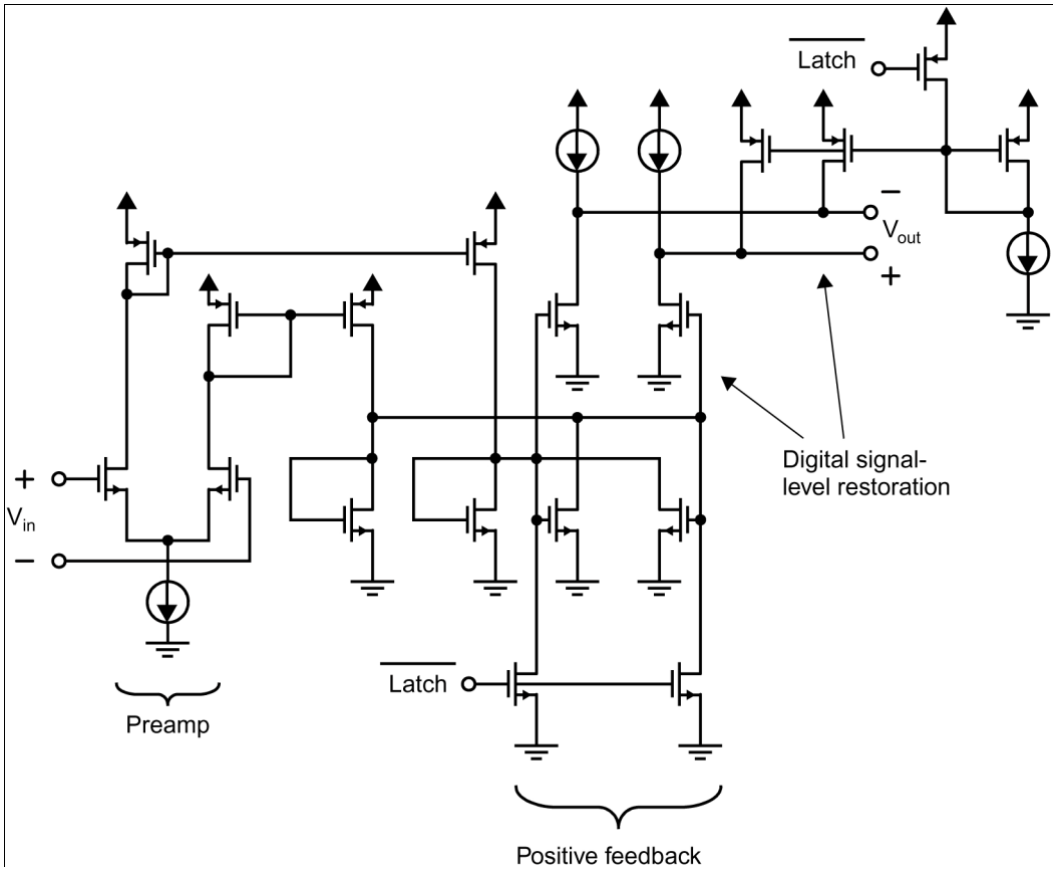
The pre-amp is implemented using diode-connected transistors, which gives small gain in order to maximize speed while still buffering the kickback away from the input circuitry.



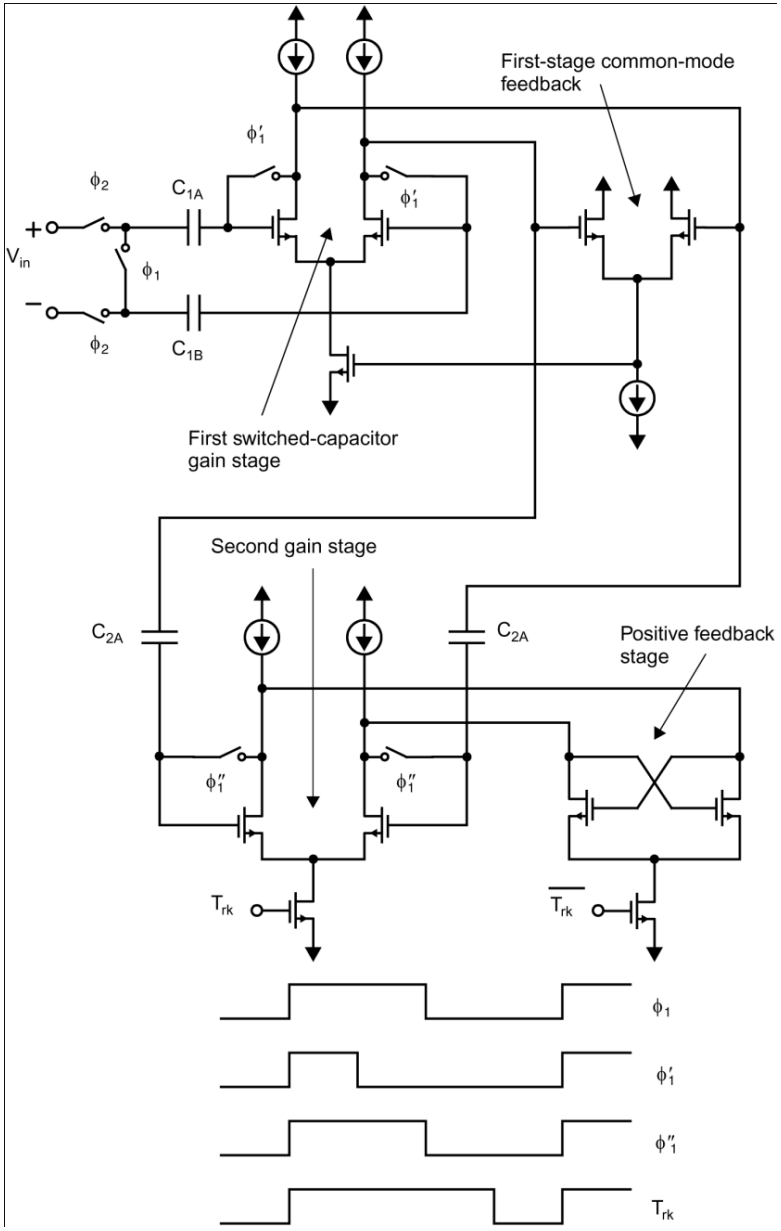
Chapter 10 Figure 20

This design also uses diode-connected loads to keep all nodes at low impedances to speed up operation.

It also uses pre-charging to eliminated any memory from the previous decision that might lead to hysteresis.



Chapter 10 Figure 21

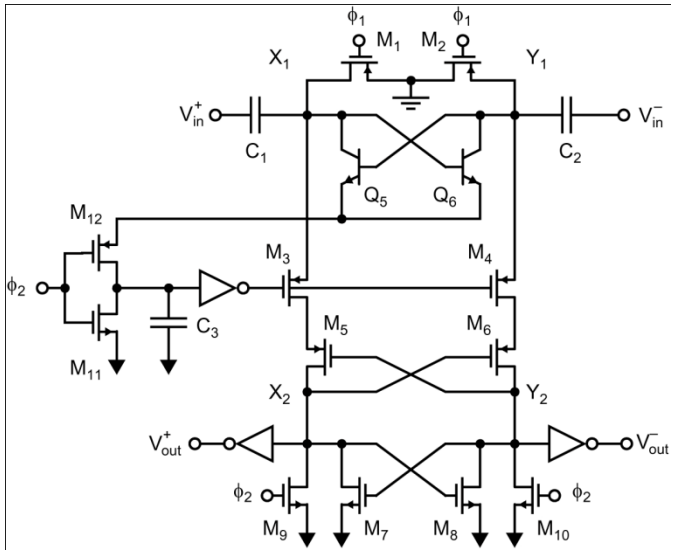


Chapter 10 Figure 22

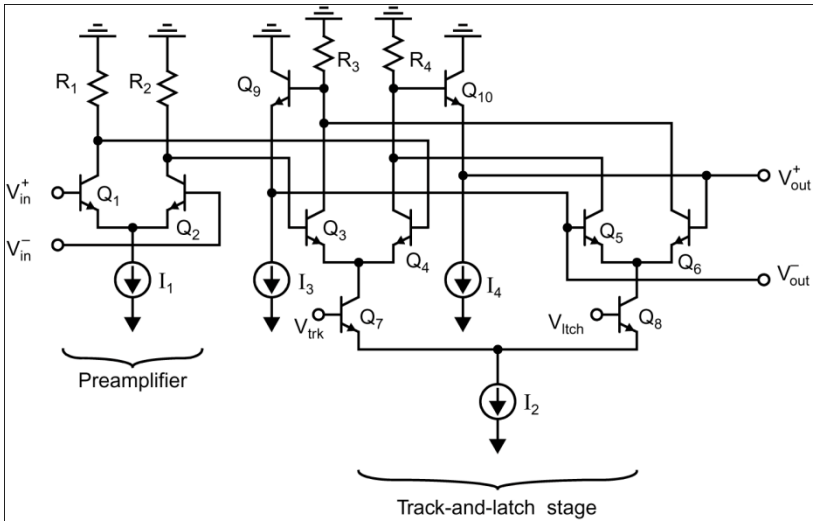
This design eliminates any input offset voltage from both the first and second stages by using capacitive coupling.

It also has common-mode feedback circuitry for the first pre-amp stage. Here the CMFB is not critical as in fully-differential OpAmps, as we only need to resolve the sign of the signal and nonlinearity is not a major issue.

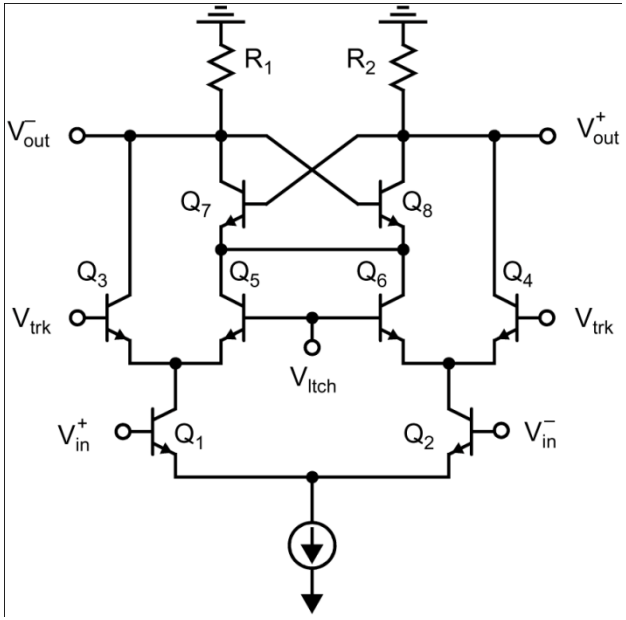
Comparators designed using BiCMOS and Bipolar technologies are popular too.



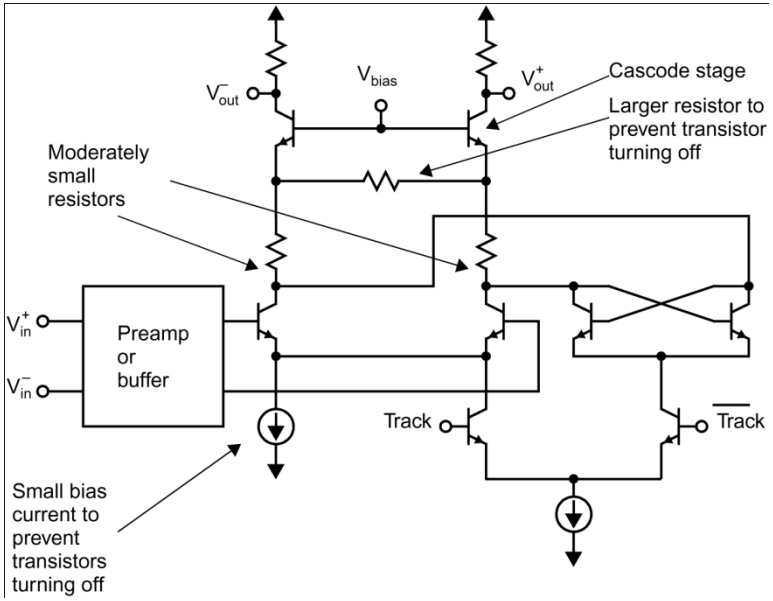
Chapter 10 Figure 23



Chapter 10 Figure 27



Chapter 10 Figure 28



Chapter 10 Figure 29

10.5.1 Input transistor charge trapping

When realizing very accurate CMOS comparators, an error mechanism that must be considered is charge trapping in the gate oxide of the input transistors.

For example, when nMOS transistors are stressed with large positive gate voltages, electrons become trapped via a tunneling mechanism but only get released after a long time in the order of milli-seconds. During this time, the effective transistor threshold voltage is increased, which leads to a comparator hysteresis on the order of 0.1 to 1mV in today's technology.

In fact, this effect correlates well with 1/f noise and is much smaller for pMOS.

So, use pMOS when realizing very accurate comparators. An alternative approach is to flush the input transistors after each cycle where the junctions and wells of nMOS are connected to a positive power supply whereas the gate connected to a negative power supply. This effectively eliminates the trapped electrons.

In addition, one can use two input stages for the comparator, one for large signals and one for small signals.