

ECEN720: High-Speed Links Circuits and Systems Spring 2021

Lecture 5: Termination, TX Driver, & Multiplexer Circuits



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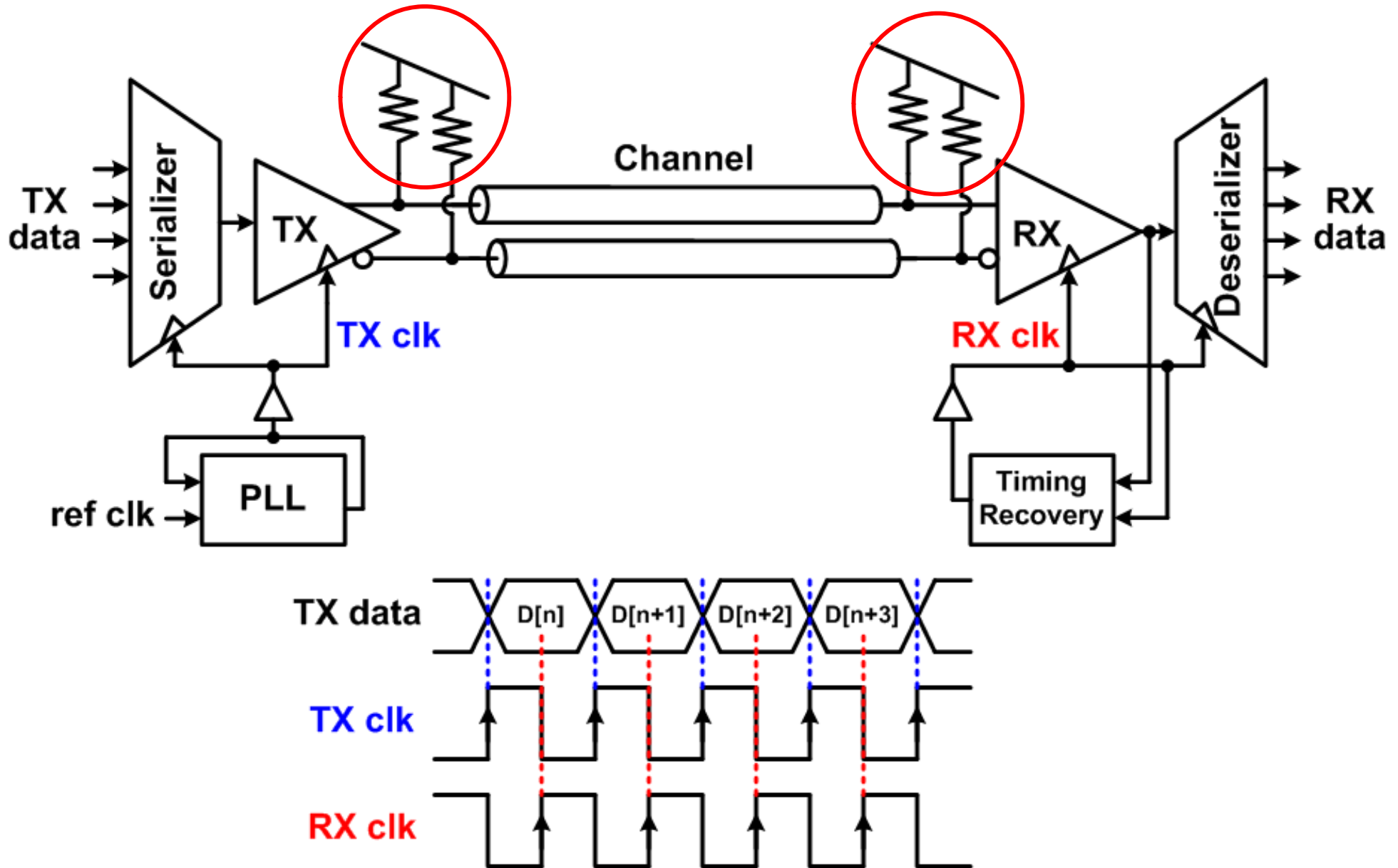
Announcements

- Lab 3 Report and Prelab 4 due Feb. 26
- Reading
 - Papers posted on voltage-mode drivers and high-order TX multiplexer circuits

Agenda

- Termination Circuits
- TX Driver Circuits
- TX circuit speed limitations
 - Clock distribution
 - Multiplexing techniques

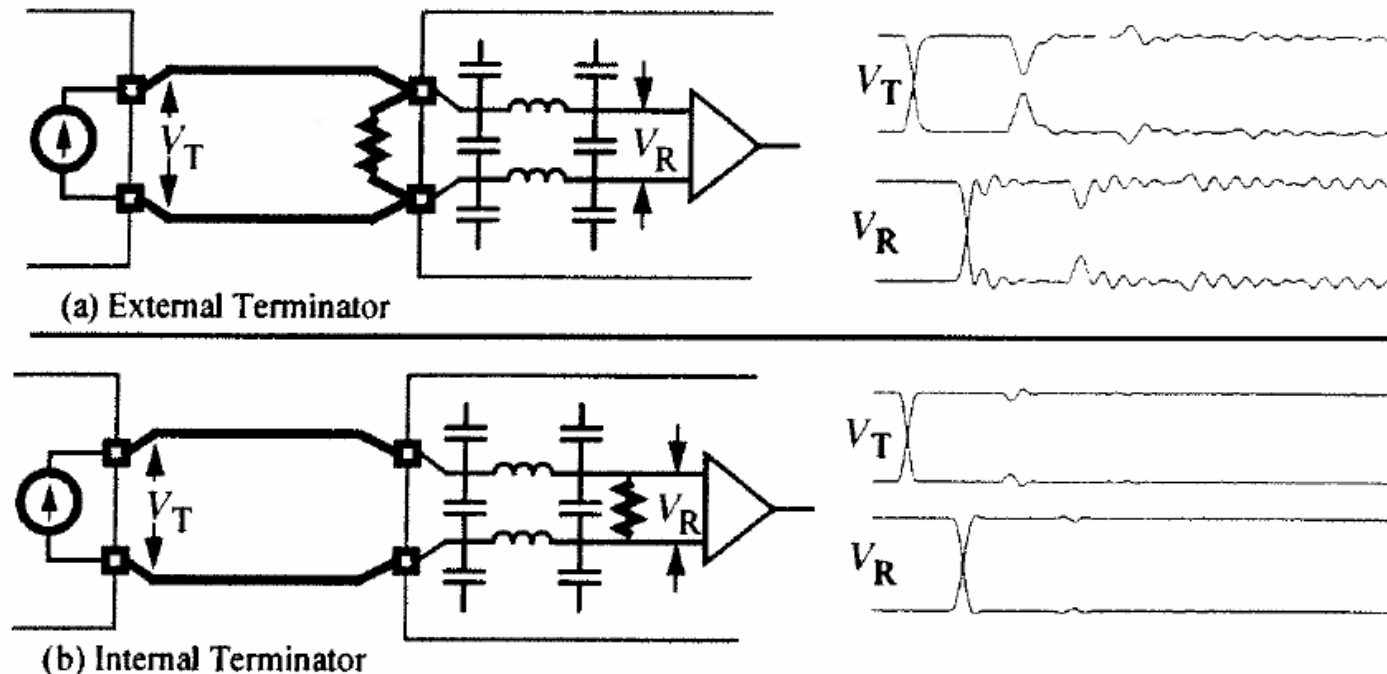
High-Speed Electrical Link System



Termination

- Off-chip vs on-chip
- Series vs parallel
- DC vs AC Coupling
- Termination circuits

Off-Chip vs On-Chip Termination

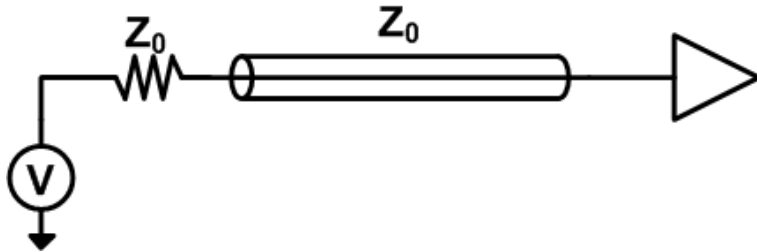


[Dally]

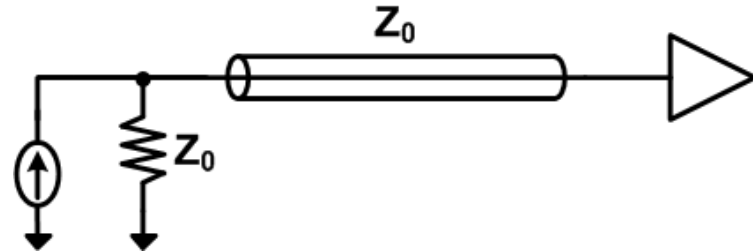
- Package parasitics act as an unterminated stub which sends reflections back onto the line
- On-chip termination makes package inductance part of transmission line

Series vs Parallel Termination

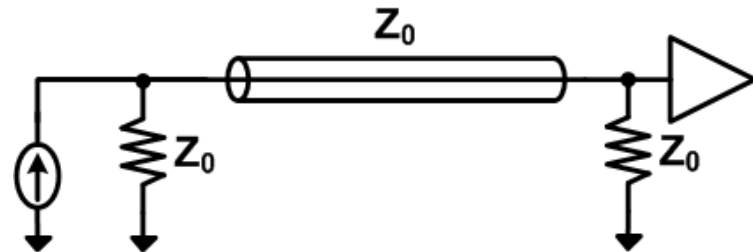
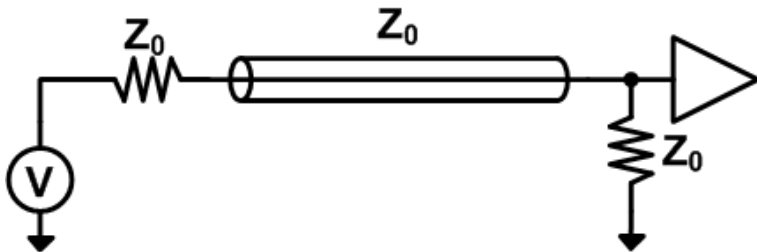
Series Termination



Parallel Termination



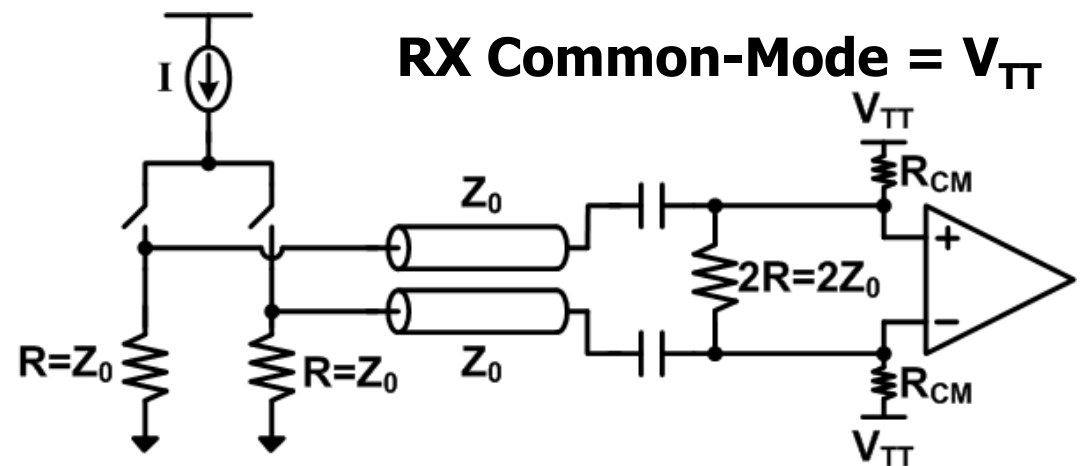
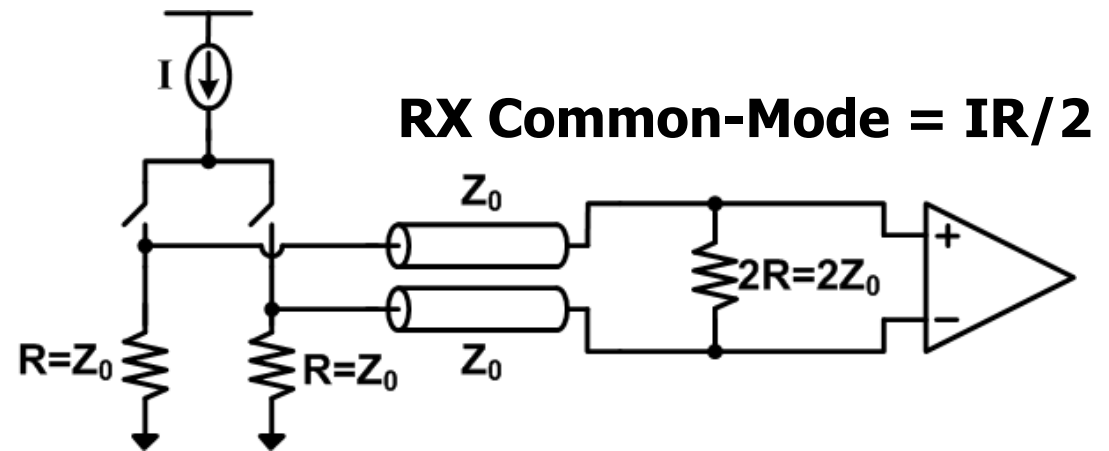
Double Termination



- Low impedance voltage-mode driver typically employs series termination
- High impedance current-mode driver typically employs parallel termination
- Double termination yields best signal quality
 - Done in majority of high performance serial links

AC vs DC Coupled Termination

- DC coupling allows for uncoded data
- RX common-mode set by transmitter signal level
- AC coupling allows for independent RX common-mode level
- Now channel has low frequency cut-off
 - Data must be coded



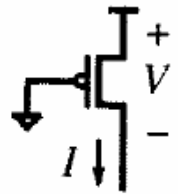
Passive Termination

- Choice of integrated resistors involves trade-offs in manufacturing steps, sheet resistance, parasitic capacitance, linearity, and ESD tolerance
- Integrated passive termination resistors are typically realized with unsalicided poly, diffusion, or n-well resistors
- Poly resistors are typically used due to linearity and tighter tolerances, but they typically vary +/-30% over process and temperature

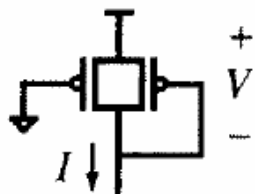
Resistor Options (90nm CMOS)

Resistor	Poly	N-diffusion	N-well
Sheet R (Ω/sq)	90 \pm 10	300 \pm 50	450 \pm 200
VC1(V ⁻¹)	0	10 ⁻³	8x10 ⁻³
Parasitic Cap	2-3fF/ μm^2 (min L poly)	0.9fF/ μm^2 (area), 0.04fF/ μm (perimeter)	0.2fF/ μm^2 (area), 0.7fF/ μm (perimeter)

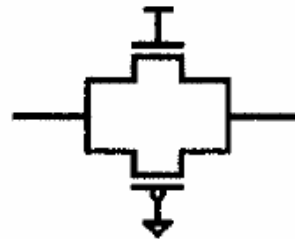
Active Termination



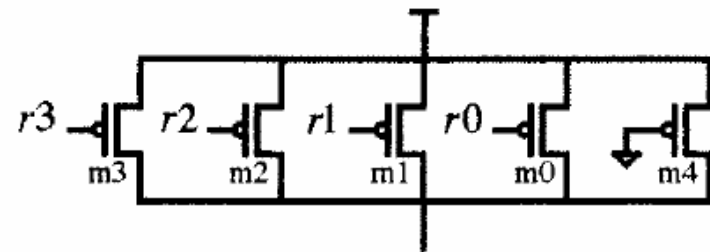
(a) Triode



(b) Two-Element



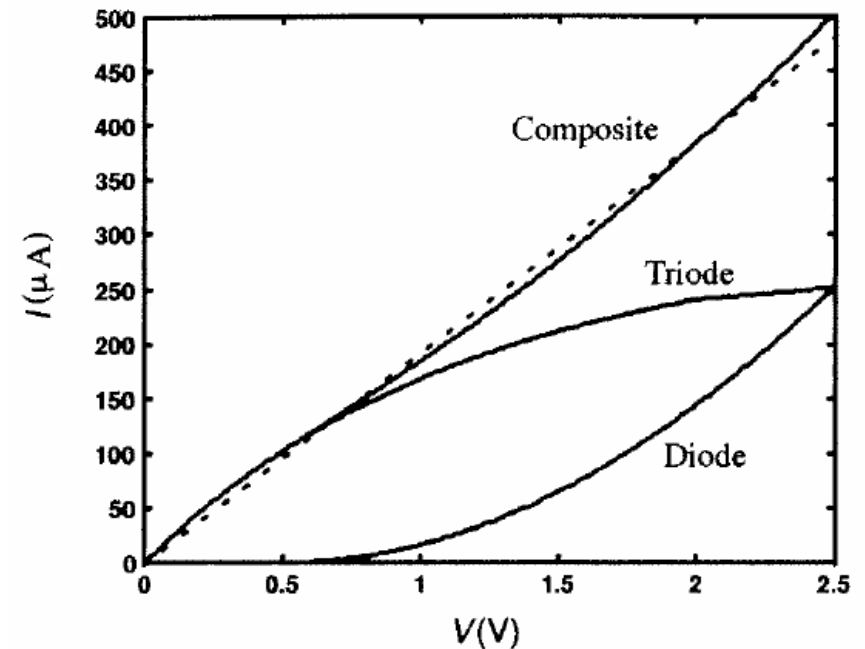
(c) Pass Gate



(d) Digital Trimming

- Transistors must be used for termination in CMOS processes which don't provide resistors
- Triode-biased FET works well for low-swing (<500mV)
 - Adding a diode connected FET increases linear range
- Pass-gate structure allows for differential termination

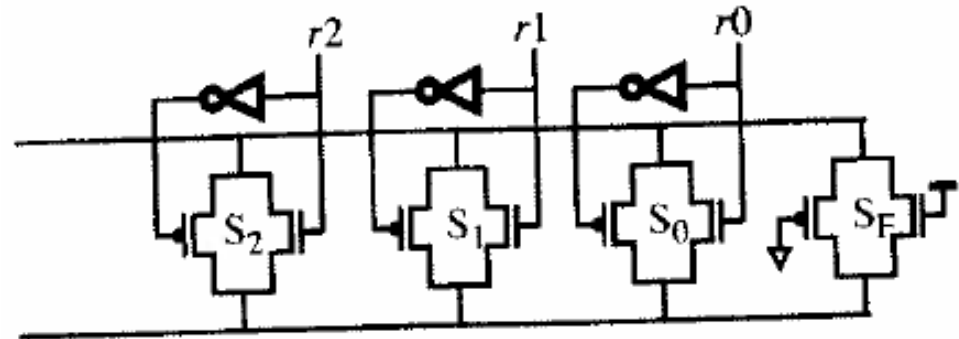
[Dally]



Adjustable Termination

- FET resistance is a function of gate overdrive

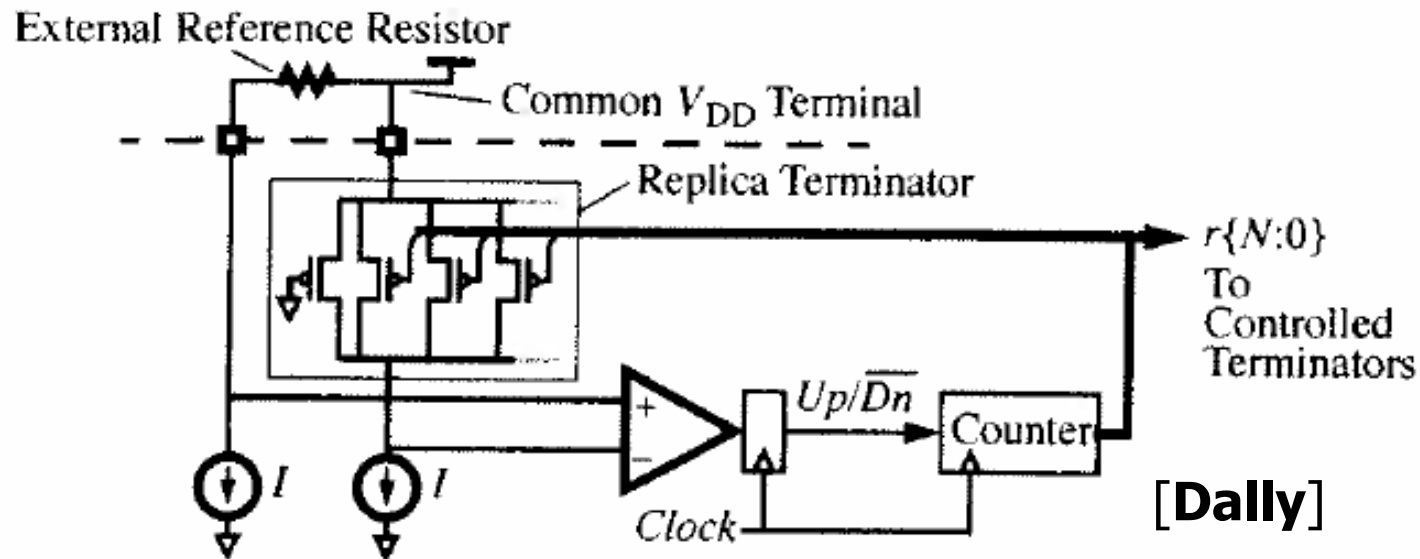
$$R_{FET} = \frac{1}{\mu C_{ox} (W/L) (V_{GS} - V_t)}$$



[Dally]

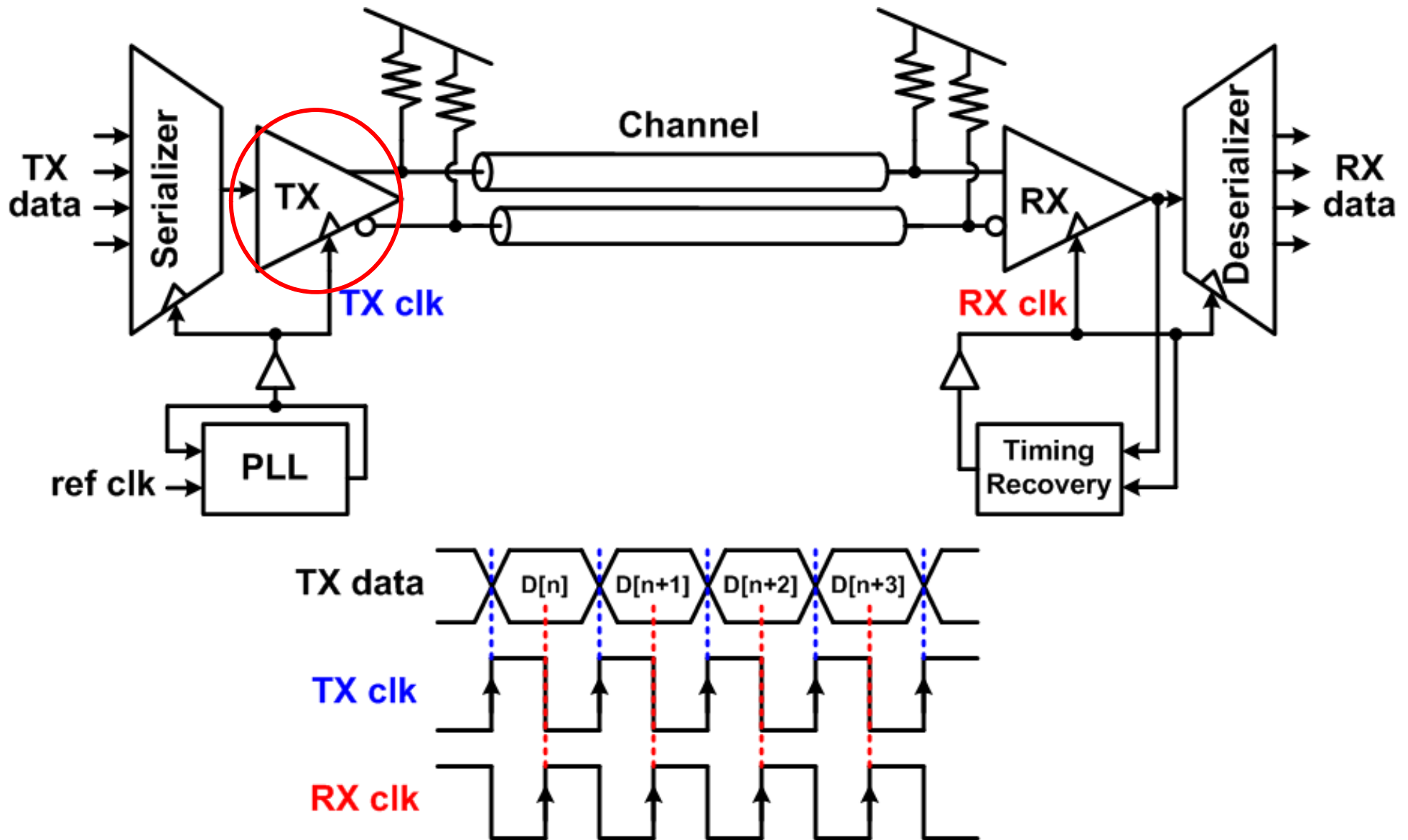
- Large variance in FET threshold voltage requires adjustable termination structures
- Calibration can be done with an analog control voltage or through digital “trimming”
 - Analog control reduces V_{GS} and linear range
 - Digital control is generally preferred

Termination Digital Control Loop



- Off-chip precision resistor is used as reference
- On-chip termination is varied until voltages are within an LSB
 - Dither filter typically used to avoid voltage noise
- Control loop may be shared among several links, but with increased nanometer CMOS variation per-channel calibration may be necessary

High-Speed Electrical Link System

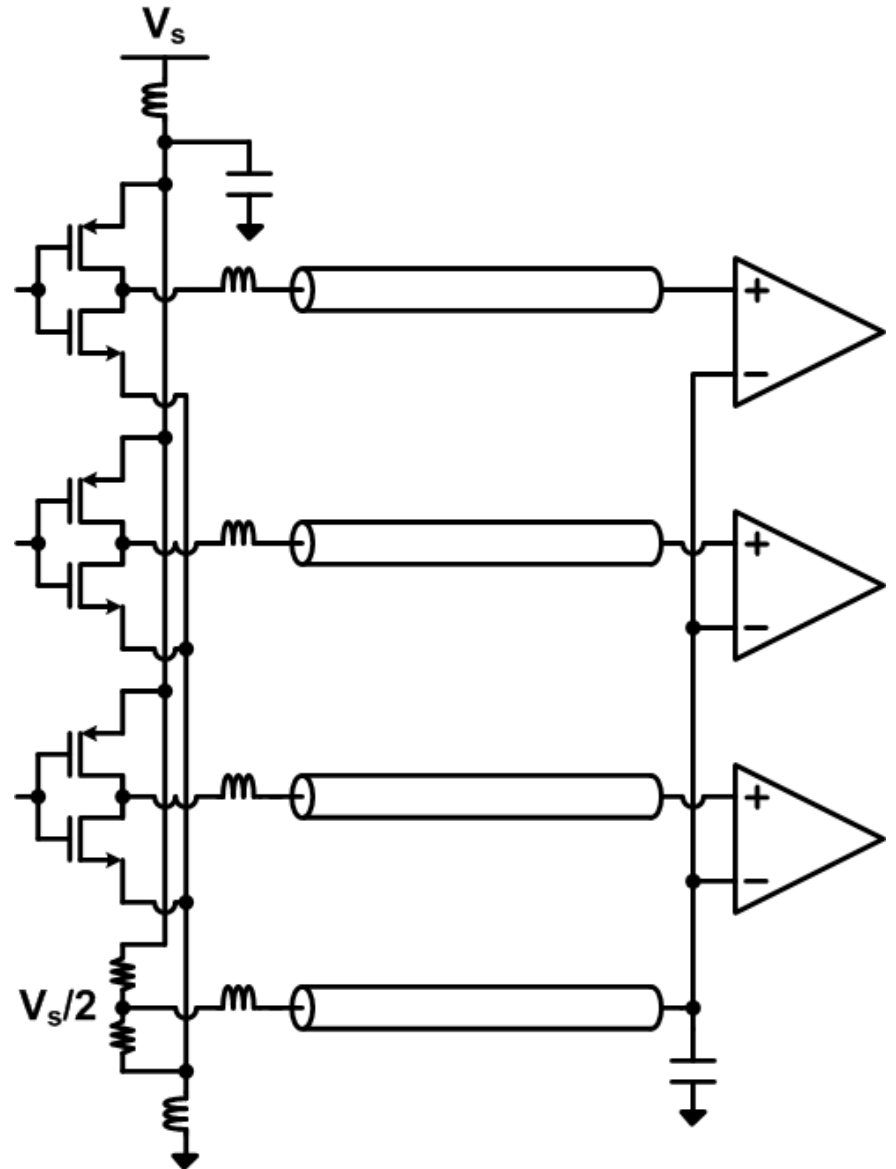


TX Driver Circuits

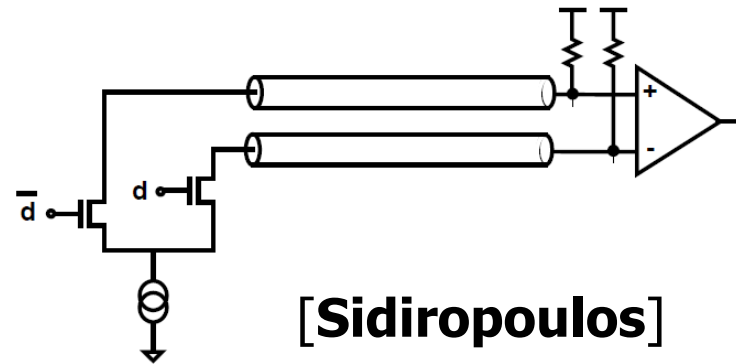
- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- Swing enhancement techniques
- Impedance control
- Pad bandwidth extension
- Slew-rate control

Single-Ended Signaling

- Finite supply impedance causes significant Simultaneous Switching Output (SSO) noise (xtalk)
- Necessitates large amounts of decoupling capacitance for supplies and reference voltage
 - Decap limits I/O area more than circuitry



Differential Signaling



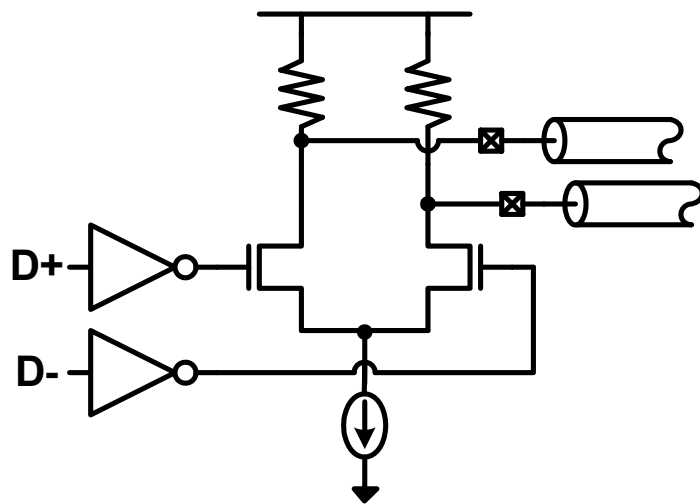
- A difference between voltage or current is sent between two lines
- Requires 2x signal lines relative to single-ended signaling, but less return pins
- Advantages
 - Signal is self-referenced
 - Can achieve twice the signal swing
 - Rejects common-mode noise
 - Return current is ideally only DC

TX Driver Circuits

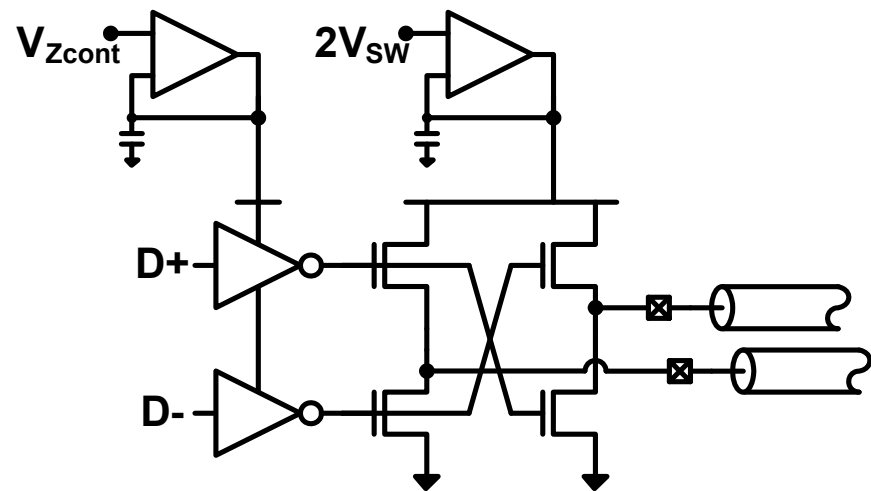
- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- Swing enhancement techniques
- Impedance control
- Pad bandwidth extension
- Slew-rate control

Controlled-Impedance Drivers

- Signal integrity considerations (min. reflections) requires 50Ω driver output impedance
- To produce an output drive voltage
 - Current-mode drivers use Norton-equivalent parallel termination
 - Easier to control output impedance
 - Voltage-mode drivers use Thevenin-equivalent series termination
 - Potentially $1/2$ to $1/4$ the current for a given output swing

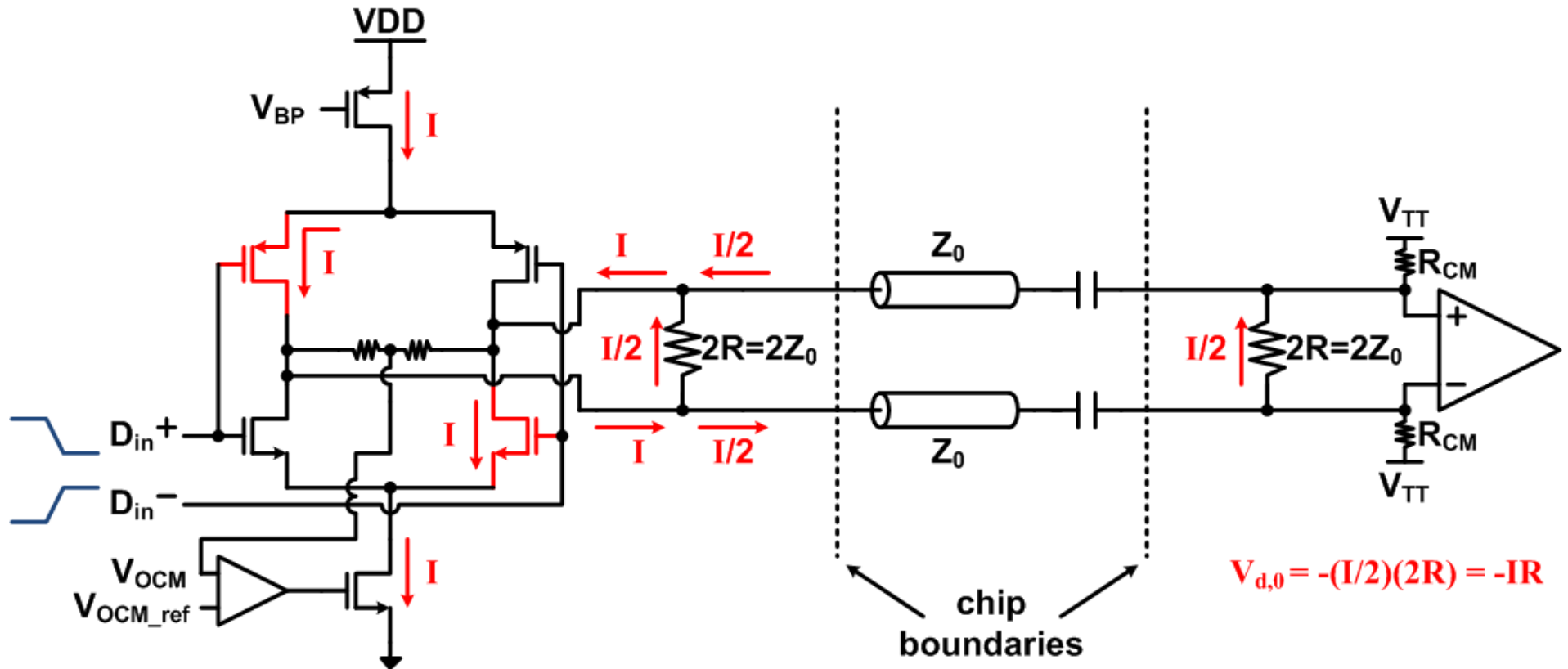


Current-Mode



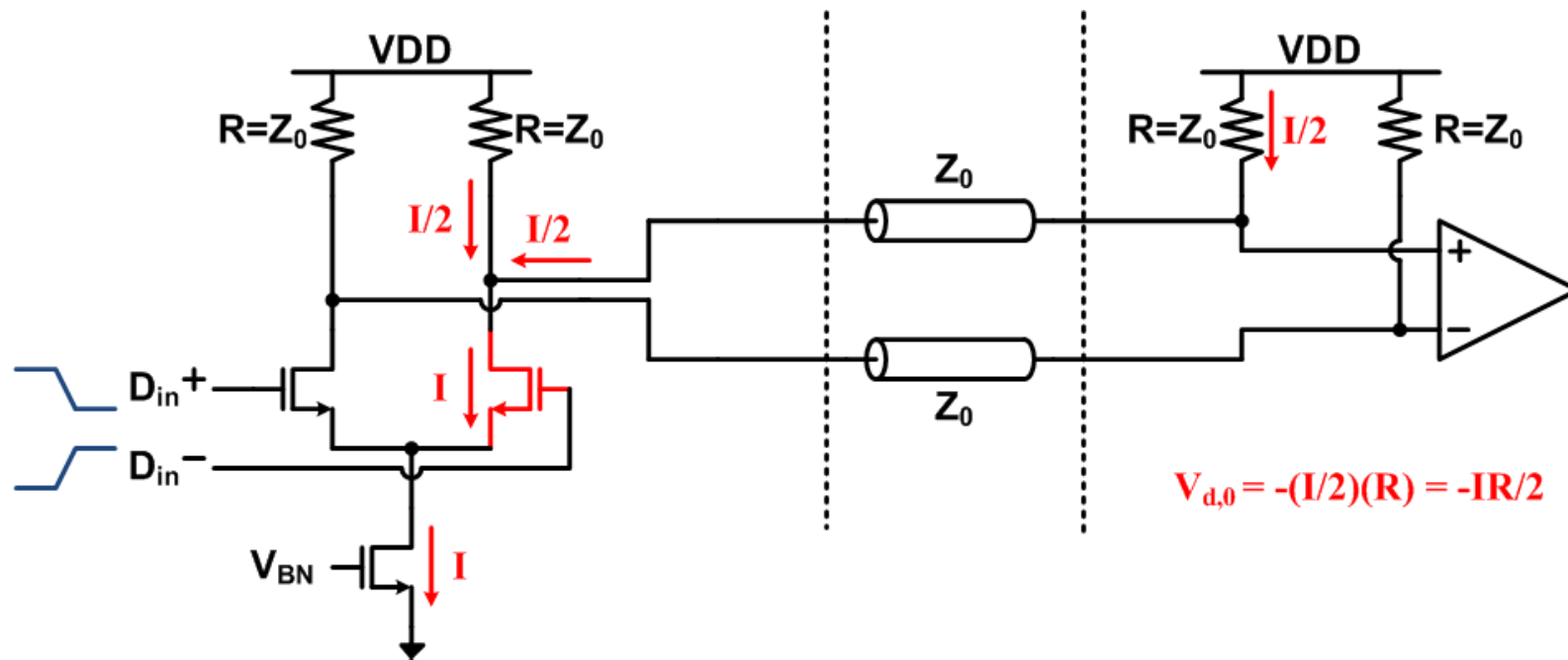
Voltage-Mode

Push-Pull Current-Mode Driver



- Used in Low-Voltage Differential Signals (LVDS) standard
- Driver current is ideally constant, resulting in low dI/dt noise
- Dual current sources allow for good PSRR, but headroom can be a problem in low-voltage technologies
- Differential peak-to-peak RX swing is $\pm IR$ with double termination

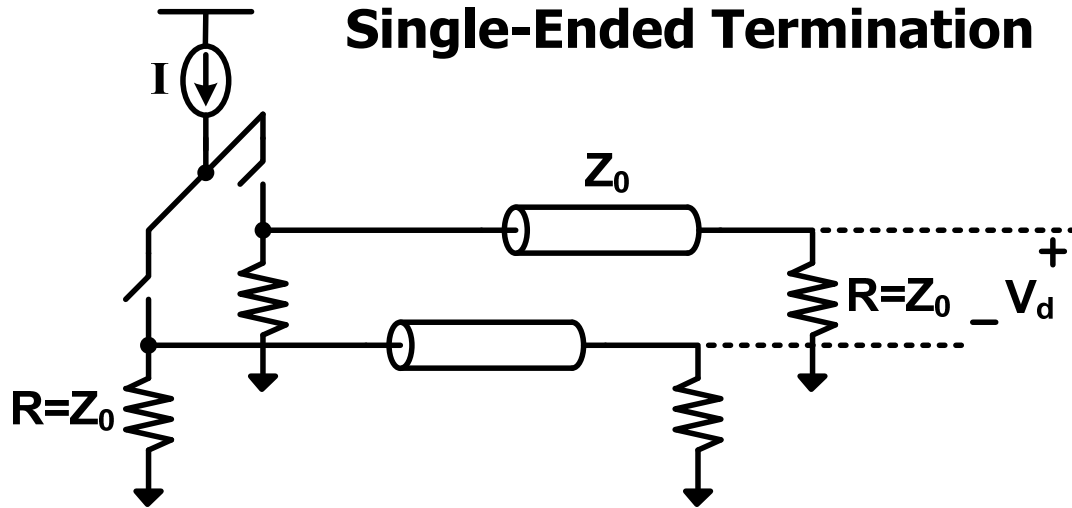
Current-Mode Logic (CML) Driver



- Used in most high performance serial links
- Low voltage operation relative to push-pull driver
 - High output common-mode keeps current source saturated
- Can use DC or AC coupling
 - AC coupling requires data coding
- Differential pp RX swing is $\pm IR/2$ with double termination

Current-Mode Current Levels

Single-Ended Termination



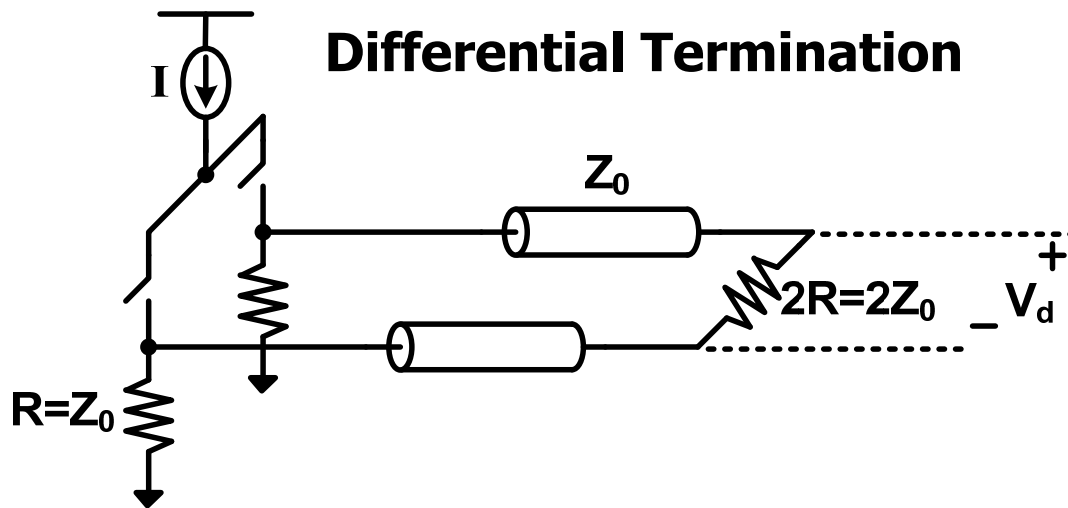
$$V_{d,1} = (I/2)R$$

$$V_{d,0} = -(I/2)R$$

$$V_{d,pp} = IR$$

$$I = \frac{V_{d,pp}}{R}$$

Differential Termination



$$V_{d,1} = (I/4)(2R)$$

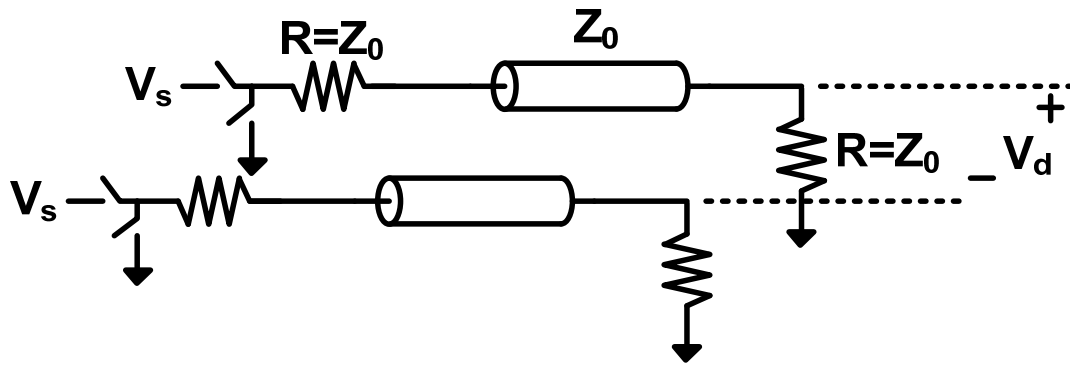
$$V_{d,0} = -(I/4)(2R)$$

$$V_{d,pp} = IR$$

$$I = \frac{V_{d,pp}}{R}$$

Voltage-Mode Current Levels

Single-Ended Termination



$$V_{d,1} = (V_s/2)$$

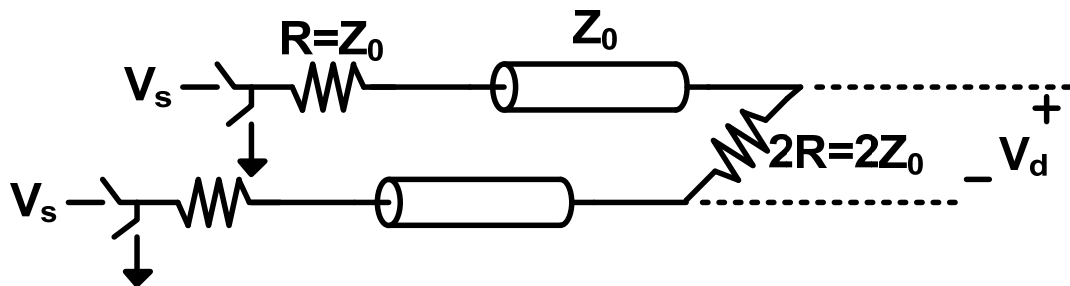
$$V_{d,0} = -(V_s/2)$$

$$V_{d,pp} = V_s$$

$$I = (V_s/2R)$$

$$I = \frac{V_{d,pp}}{2R}$$

Differential Termination



$$V_{d,1} = (V_s/2)$$

$$V_{d,0} = -(V_s/2)$$

$$V_{d,pp} = V_s$$

$$I = (V_s/4R)$$

$$I = \frac{V_{d,pp}}{4R}$$

Current-Mode vs Voltage-Mode Summary

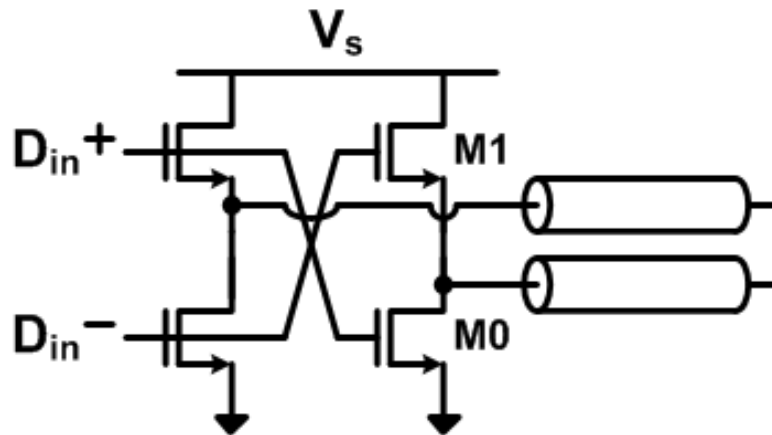
Driver/Termination	Current Level	Normalized Current Level
Current-Mode/SE	$V_{d,pp}/Z_0$	1x
Current-Mode/Diff	$V_{d,pp}/Z_0$	1x
Voltage-Mode/SE	$V_{d,pp}/2Z_0$	0.5x
Voltage-Mode/Diff	$V_{d,pp}/4Z_0$	0.25x

- An ideal voltage-mode driver with differential RX termination enables a *potential* 4x reduction in driver power
- *Actual* driver power levels also depend on
 - Output impedance control
 - Pre-driver power
 - Equalization implementation

Voltage-Mode Drivers

- Voltage-mode driver implementation depends on output swing requirements
- For low-swing (<400-500mVpp), an all NMOS driver is suitable
- For high-swing, CMOS driver is used

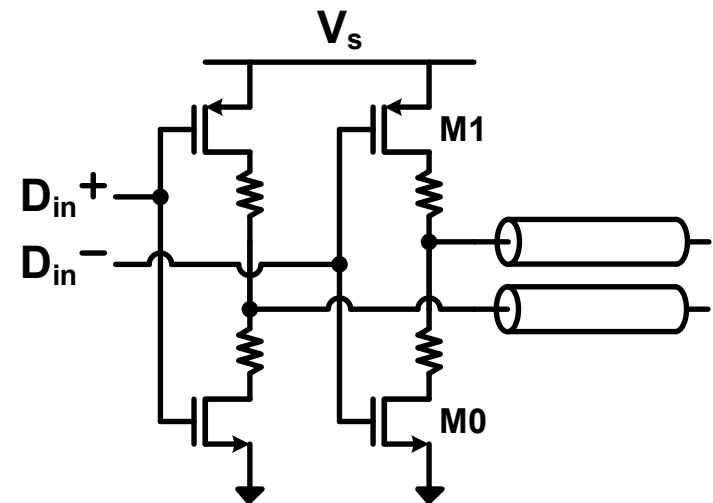
Low-Swing Voltage-Mode Driver



$$V_s < \frac{4}{3}(V_{DD} - V_{t1} - V_{OD1}) \text{ (Diff. Term)}$$

$$V_s < 2(V_{DD} - V_{t1} - V_{OD1}) \text{ (SE Term)}$$

High-Swing Voltage-Mode Driver



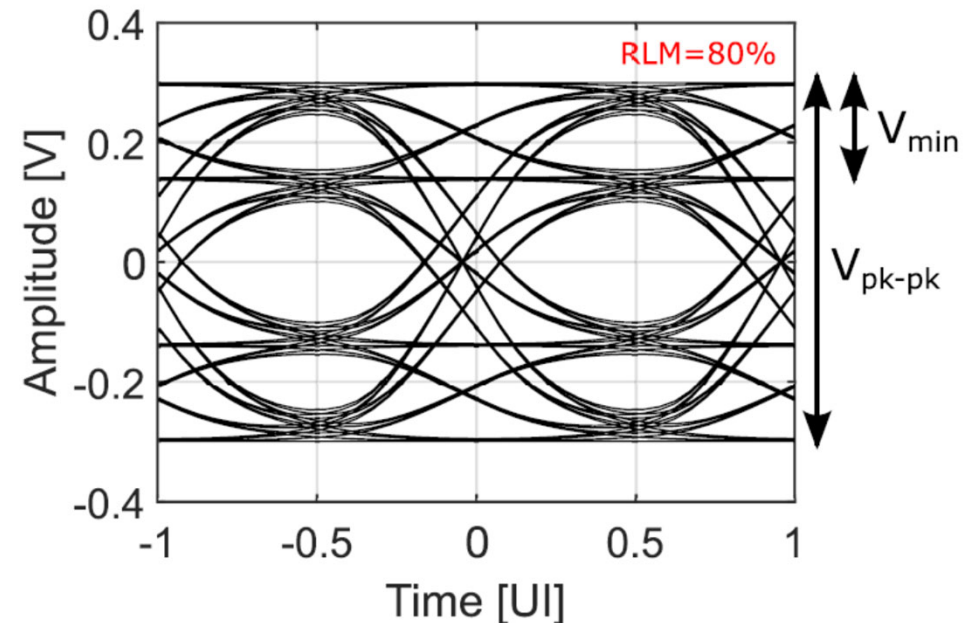
$$V_s > |V_{t1}| + V_{OD1}$$

TX Driver Circuits

- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- **Swing enhancement techniques**
- Impedance control
- Pad bandwidth extension
- Slew-rate control

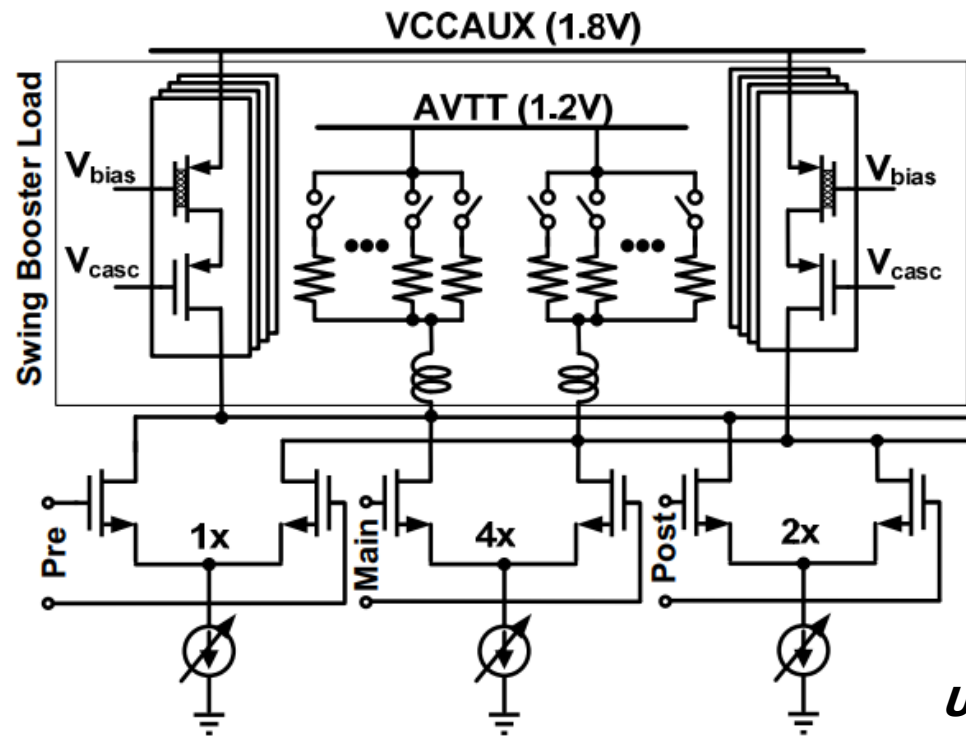
High-Swing Transmitter Linearity

- Transmit swings $\geq 1V_{ppd}$ are often needed to support operation over high-loss channels
- Reductions in supply voltages make achieving this swing with high linearity difficult
- This is particularly important with PAM4 modulation



$$RLM = 3 \frac{V_{min}}{V_{pk-pk}}$$

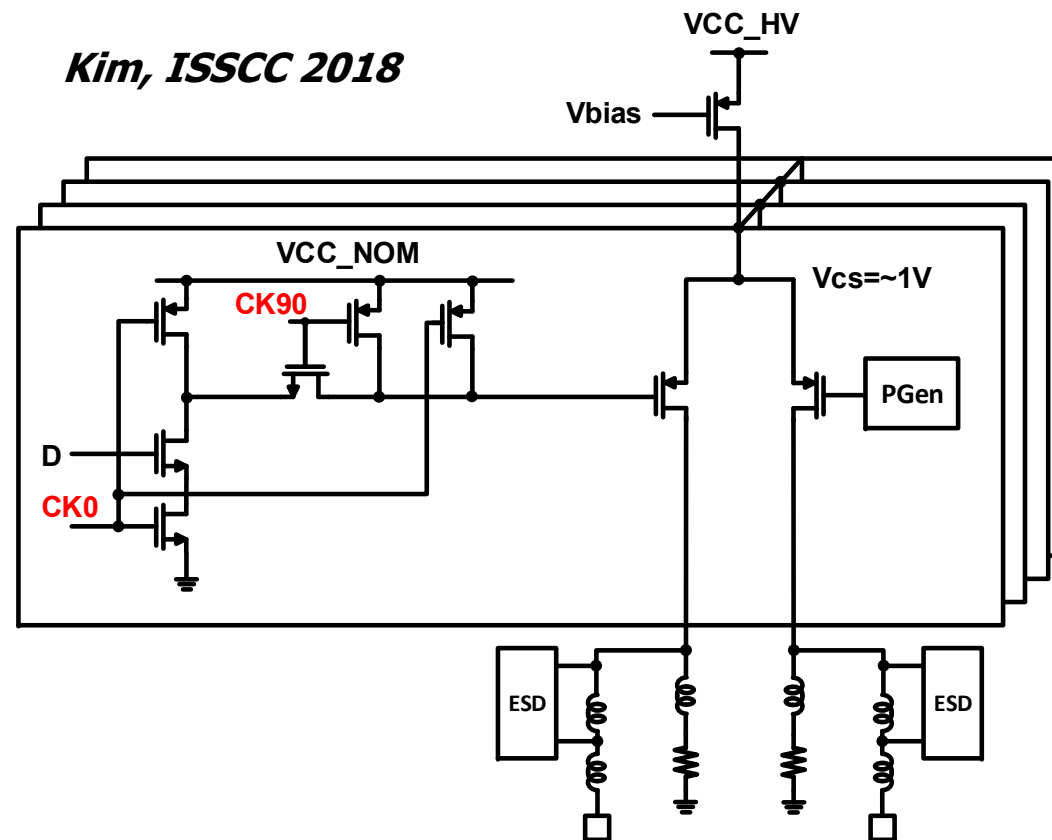
Parallel Bleeder Current Source



Upadhyaya, VLSI 2016

- Parallel thick-oxide bleeder current source from 1.8V supply raises output common mode
- Achieves $>1.2V_{ppd}$ swing in a 16nm FinFET process

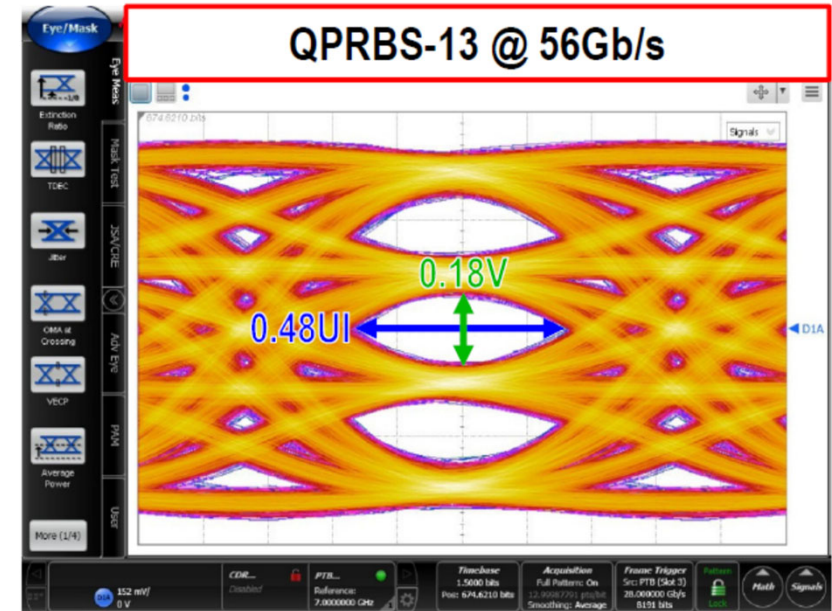
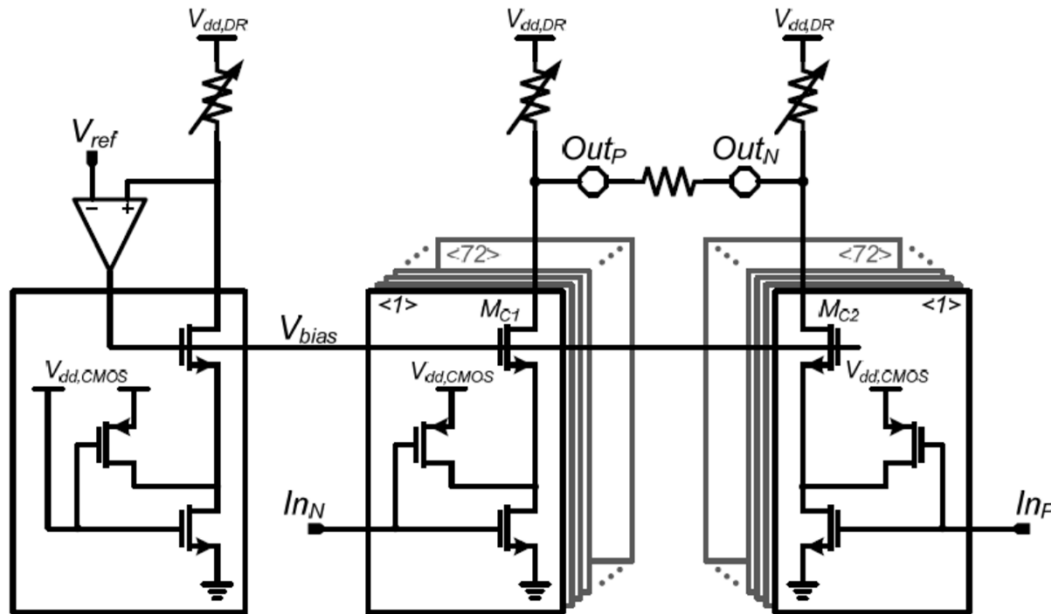
CML Driver w/ Higher Output Stage Supply



- Higher output stage supply
- Source voltage of switch PMOS transistors remains near 1V for 10nm reliability
- $>1V_{ppd}$ swing

Tail-Less Current-Mode Driver

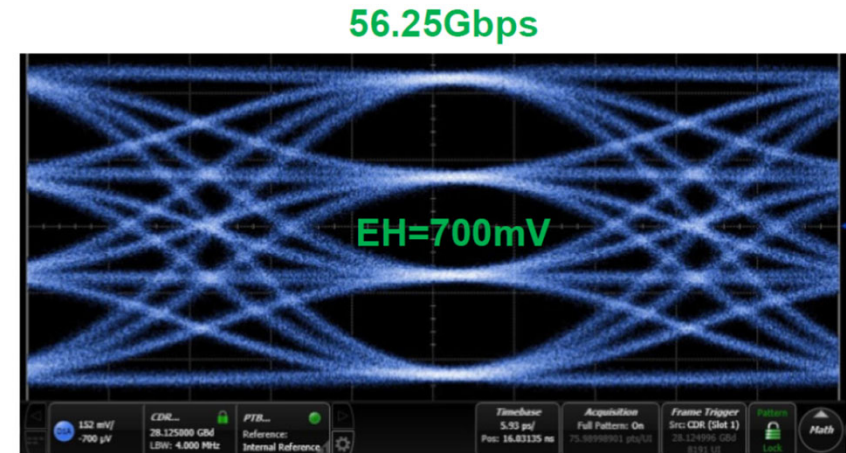
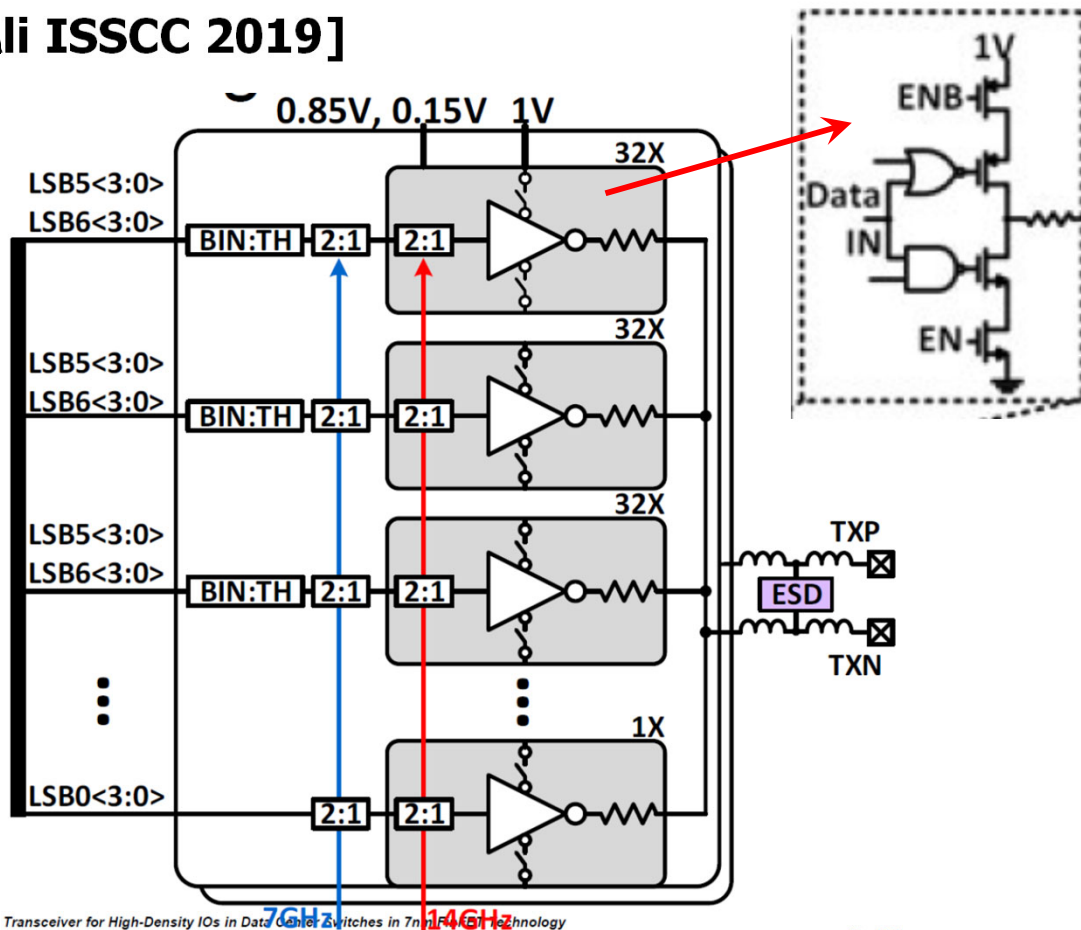
[Steffan ISSCC 2017]



- Bottom transistor driven by full-rate serialized data
- Replica-bias network sets output stage cascode transistors' gate voltage to achieve the desired output swing
- Achieves $1.2V_{ppd}$ output swing with 94% RLM

Voltage-Mode Driver w/ Level-Shifting Predriver

[Ali ISSCC 2019]



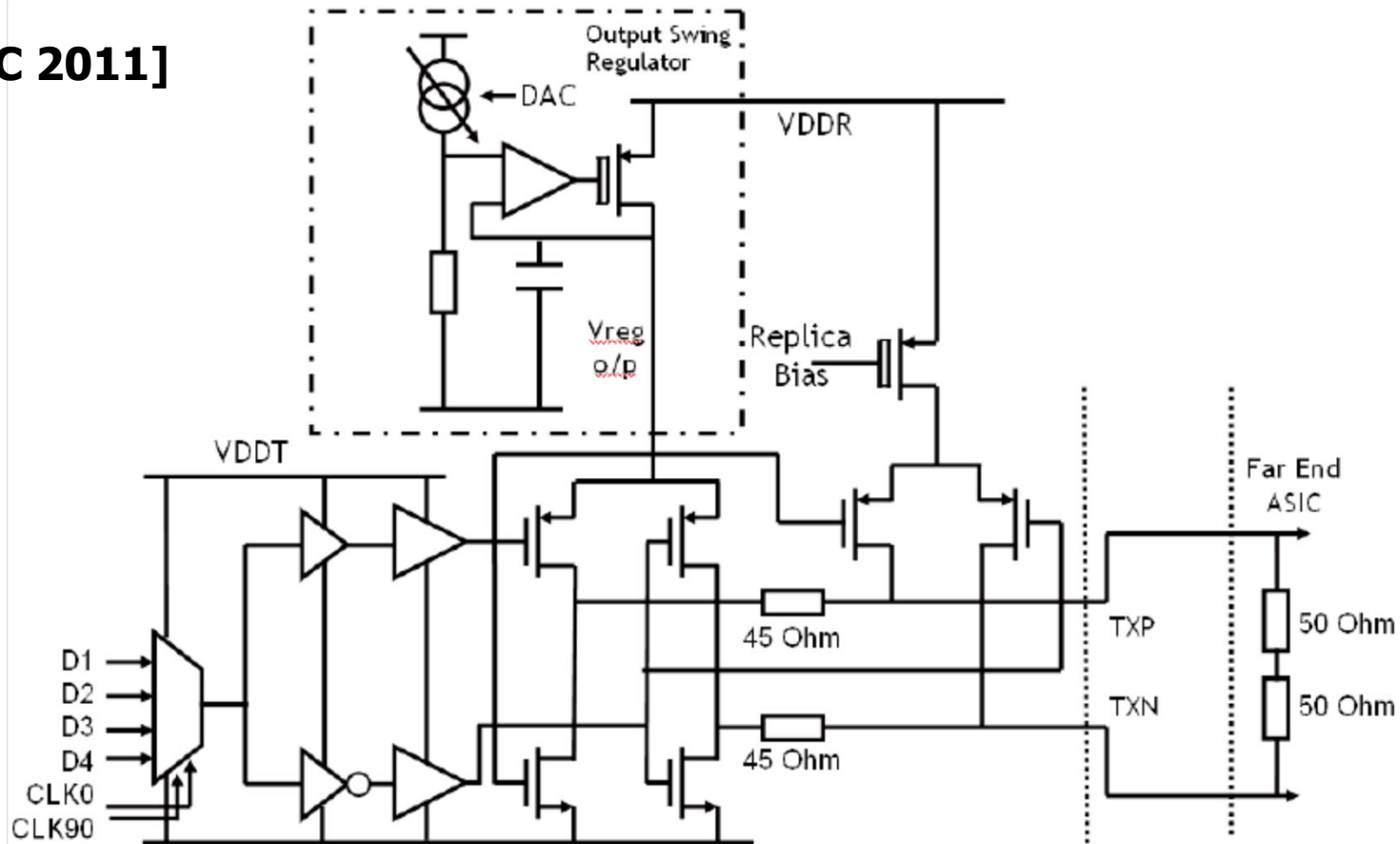
Package+PCB loss is ~3dB, FIR applied to open eye

RLM = 98.5, SNDR = 37dB, SNR_ISI = 37.7dB

- Predriver uses a 0.85V supply to drive the NMOS and a level shifted 0.15V GND to drive the PMOS
- Achieves $1V_{ppd}$ output swing in 7nm CMOS

Hybrid Voltage-Mode Driver w/ Parallel Current-Mode Segments

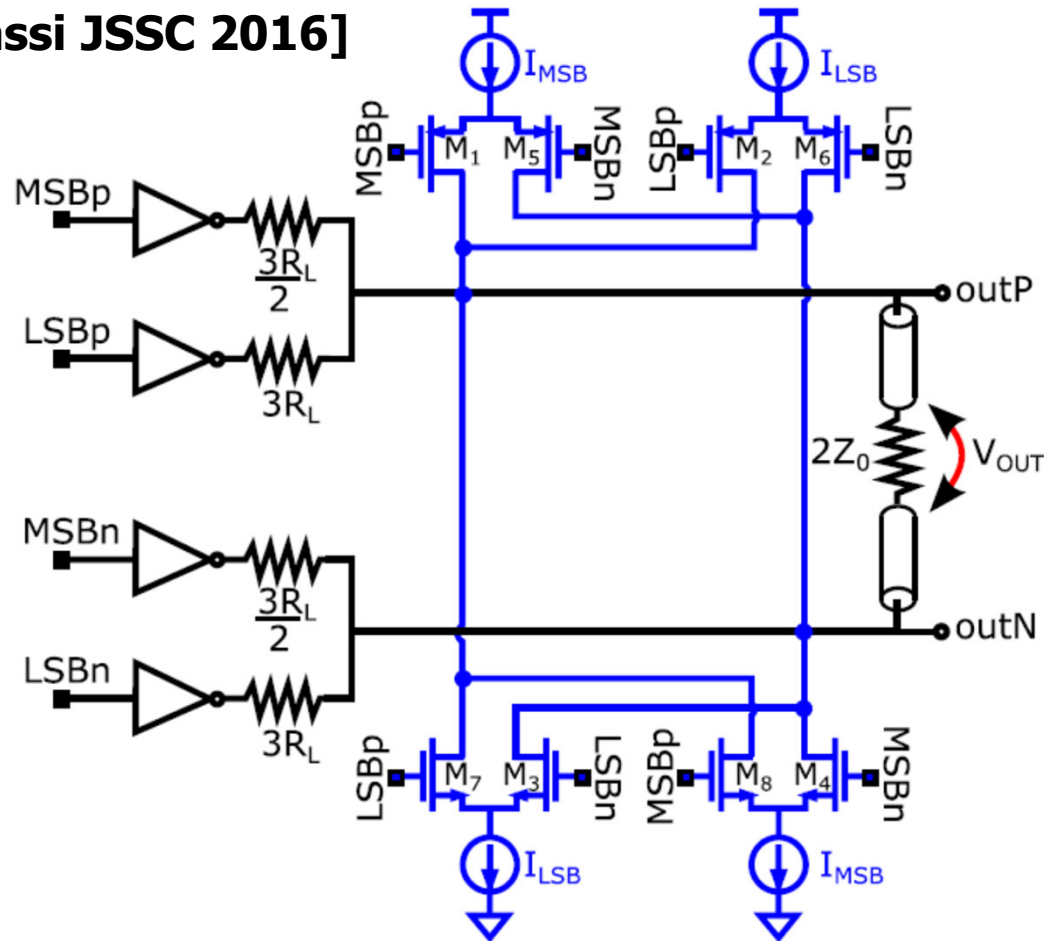
[Joy ISSCC 2011]



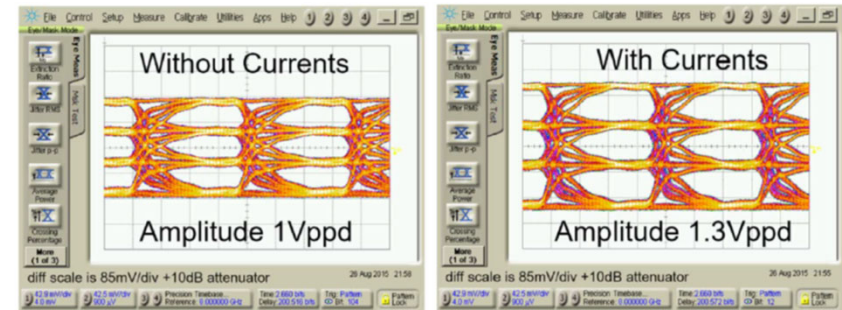
- Parallel current-mode output stage provides swing enhancement
- Achieves $1.2V_{ppd}$ output swing in 40nm CMOS

PAM4 Hybrid Voltage-Mode Driver w/ Parallel Push-Pull Current-Mode Segments

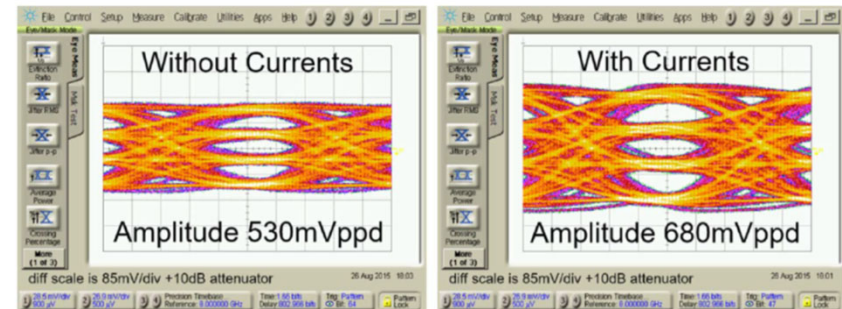
[Bassi JSSC 2016]



Low-Speed Operation



45Gb/s

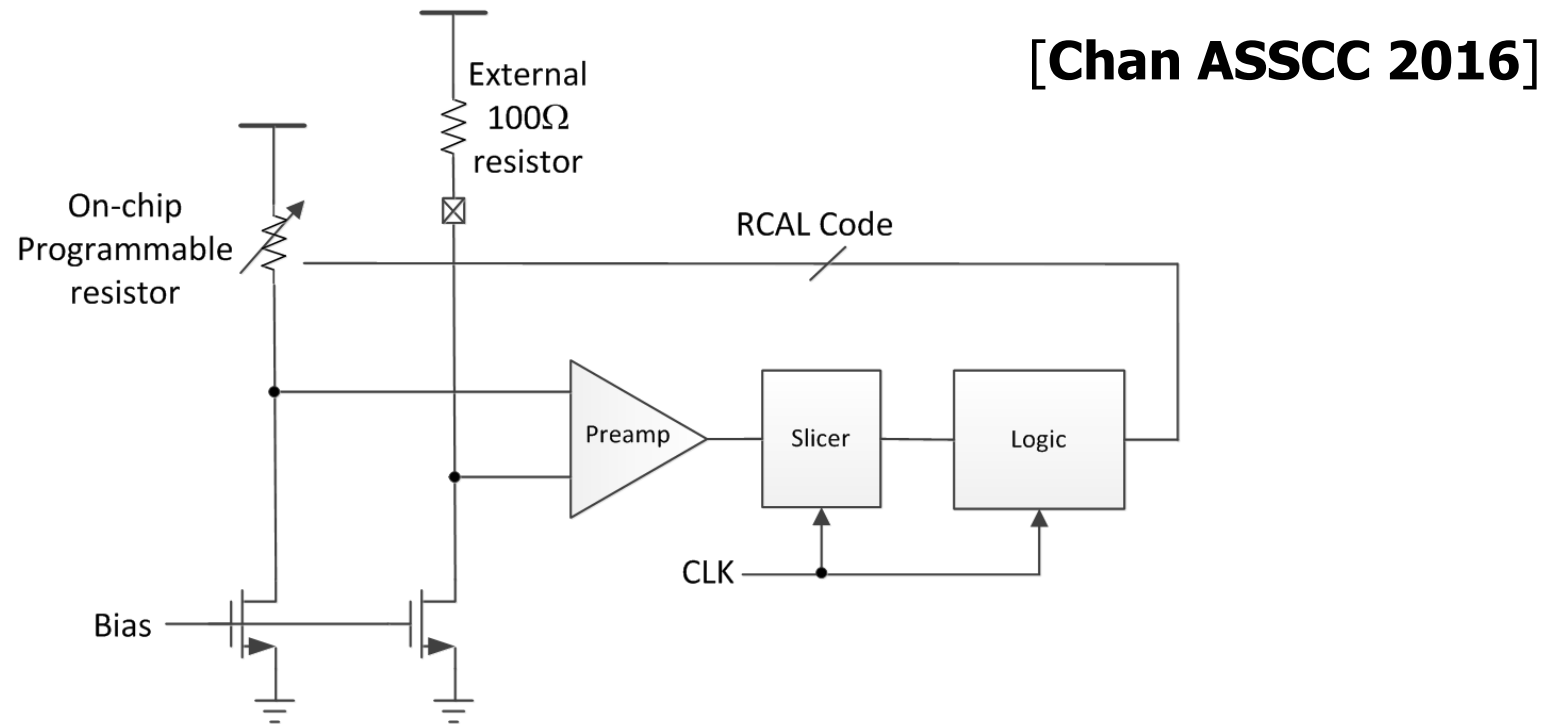


- Parallel push-pull current sources driven by the MSB & LSB allow for a high-swing PAM4 implementation
- Achieves $1.3V_{ppd}$ output swing in 1V 28nm CMOS with $>94\%$ RLM

TX Driver Circuits

- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- Swing enhancement techniques
- Impedance control
- Pad bandwidth extension
- Slew-rate control

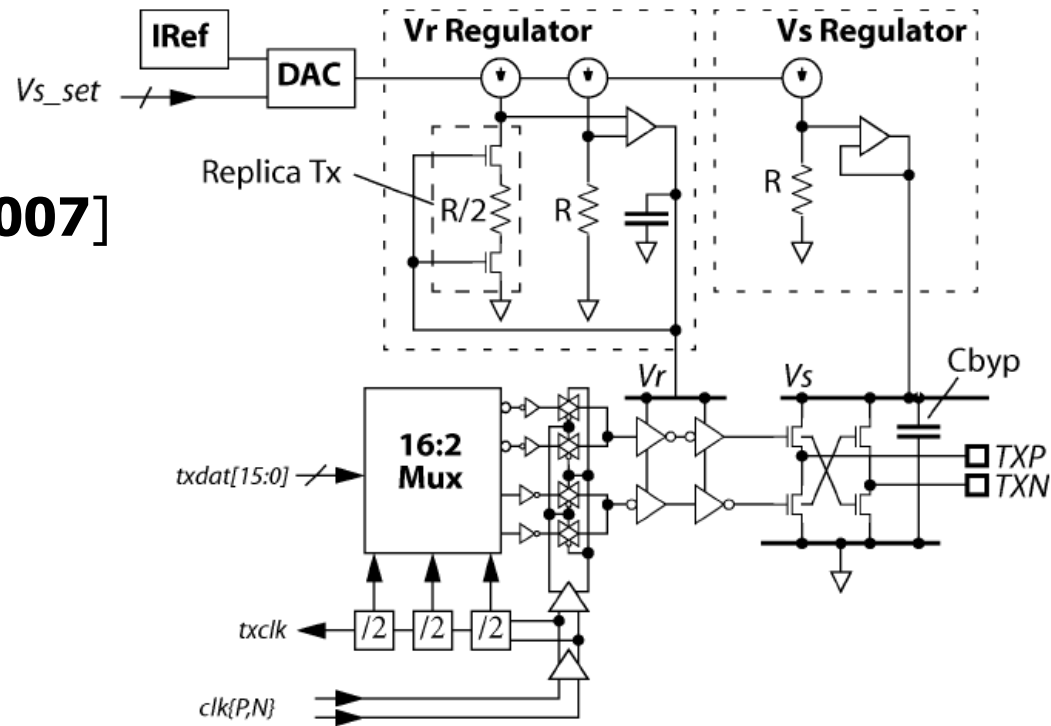
Global Resistor Calibration



- Off-chip precision resistor is used as reference
- On-chip termination is varied until voltages are within an LSB
 - Dither filter typically used to avoid voltage noise
- In current-mode drivers, this code is used for the nominal load setting

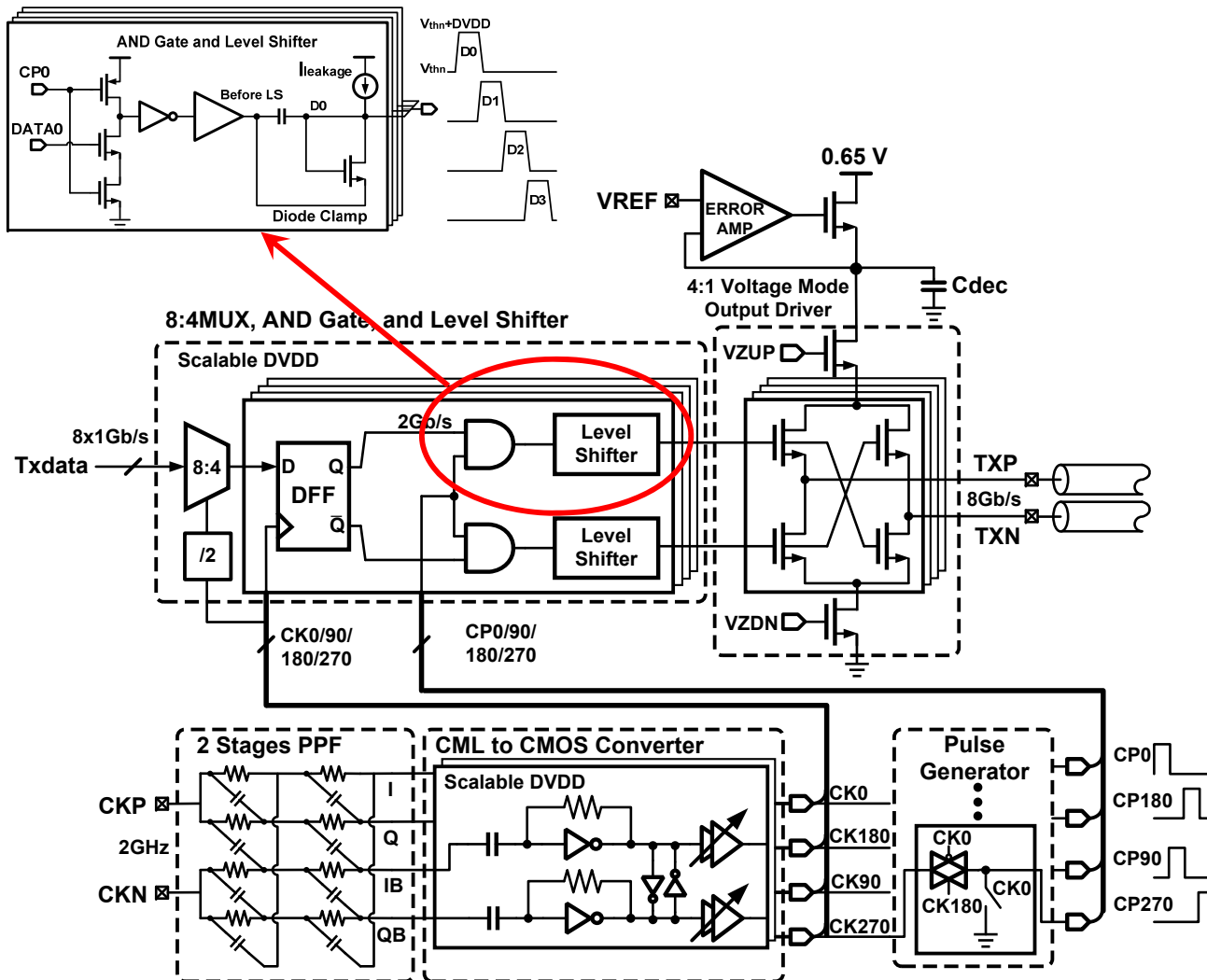
Low-Swing VM Driver Impedance Control

[Poulton JSSC 2007]



- A linear regulator sets the output stage supply, V_s
- Termination is implemented by output NMOS transistors
- To compensate for PVT and varying output swing levels, the pre-drive supply is adjusted with a feedback loop
- The top and bottom output stage transistors need to be sized differently, as they see a different V_{OD}

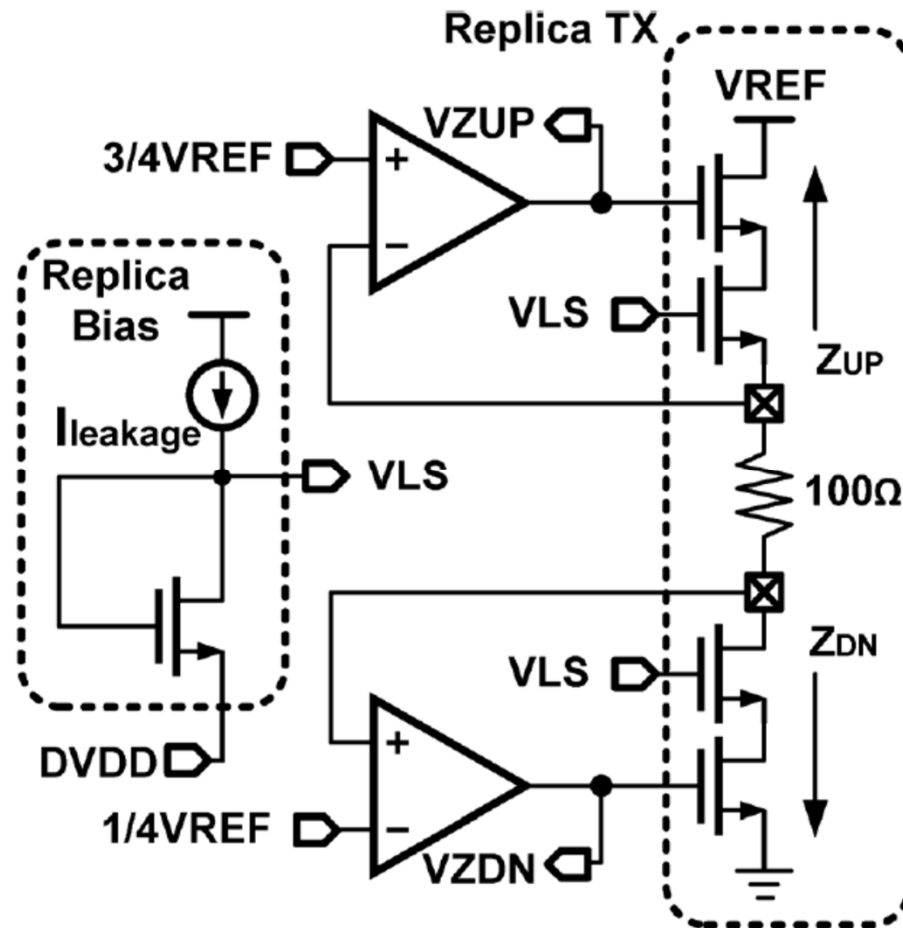
4:1 Output Multiplexing Voltage-Mode TX



- Impedance control is achieved independent of the pre-driver supply by adding additional up/down analog-controlled NMOS transistors
- Level-shifting pre-driver allows for smaller output transistors

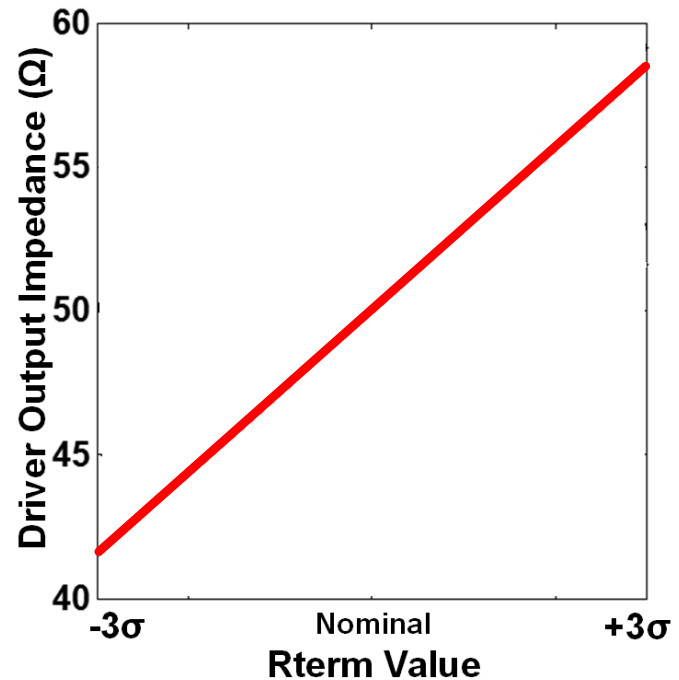
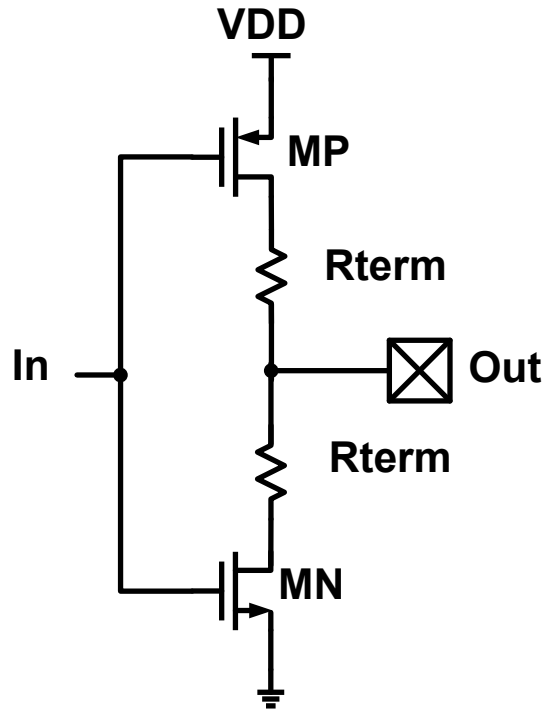
Low-Swing Voltage-Mode Driver

Analog Impedance Control



- Replica global impedance control loop provides analog gate voltages to the additional top/bottom transistors to set the pull-up/down impedance

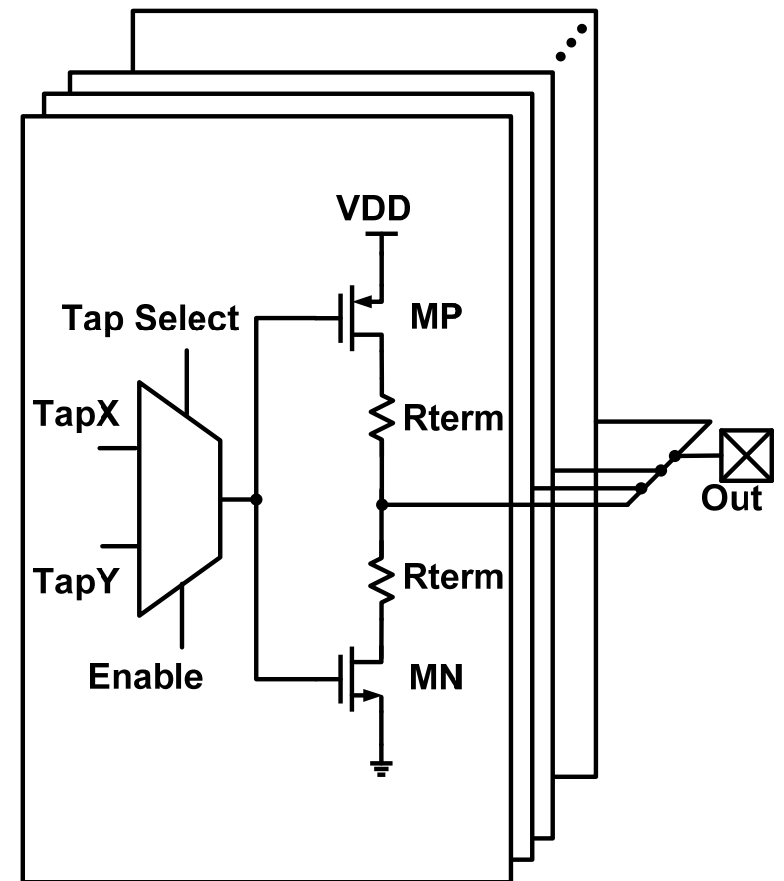
High-Swing Voltage-Mode Driver Impedance Control



- Passive resistors + transistors' triode resistance
- Output impedance will change due to process variation
- Causes reflection and level mismatch

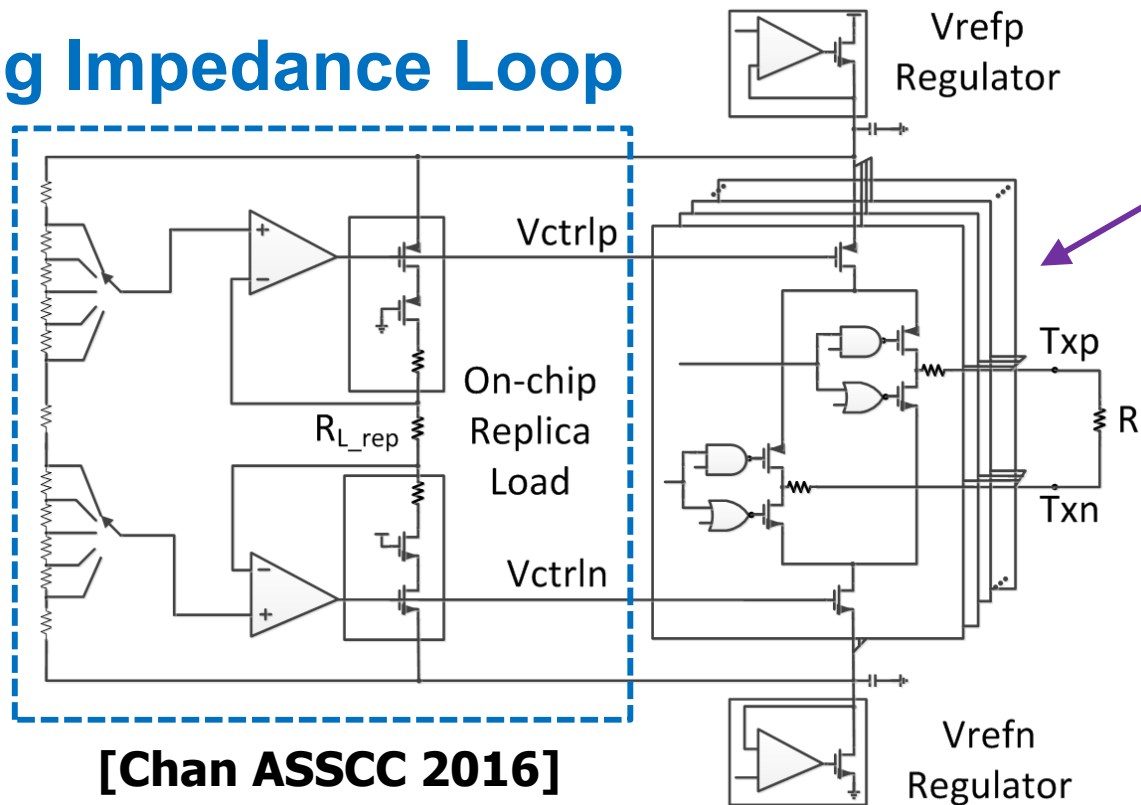
High-Swing Voltage-Mode Driver Impedance Control

- Equalization control by setting the number of segments connected to each tap
- Termination control by setting the total number of enabled segments
- Disadvantages:
 - Transistor stacking in full-rate path
 - Extra area due to redundant segments
 - Extra power consumption because pre-driver should be sized to drive maximum load
 - Sensitive to P/N skew variations



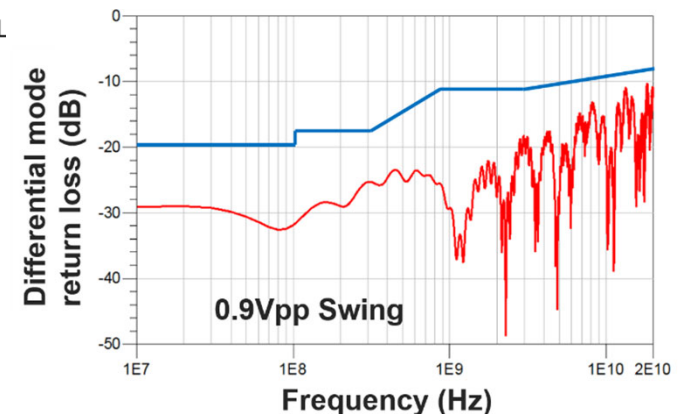
High-Swing Voltage-Mode Driver Hybrid Impedance Control Scheme

Analog Impedance Loop



[Chan ASSCC 2016]

75 to 85
driver slices
(10 programmable
slices with NAND and
NOR as pre-driver)



- Programmable number of driver slices provides coarse impedance control to compensate for resistor variations
- Analog impedance loop provides fine impedance control to compensate for NMOS/PMOS variations
- Measured differential mode return loss meets key protocols composite return loss mask

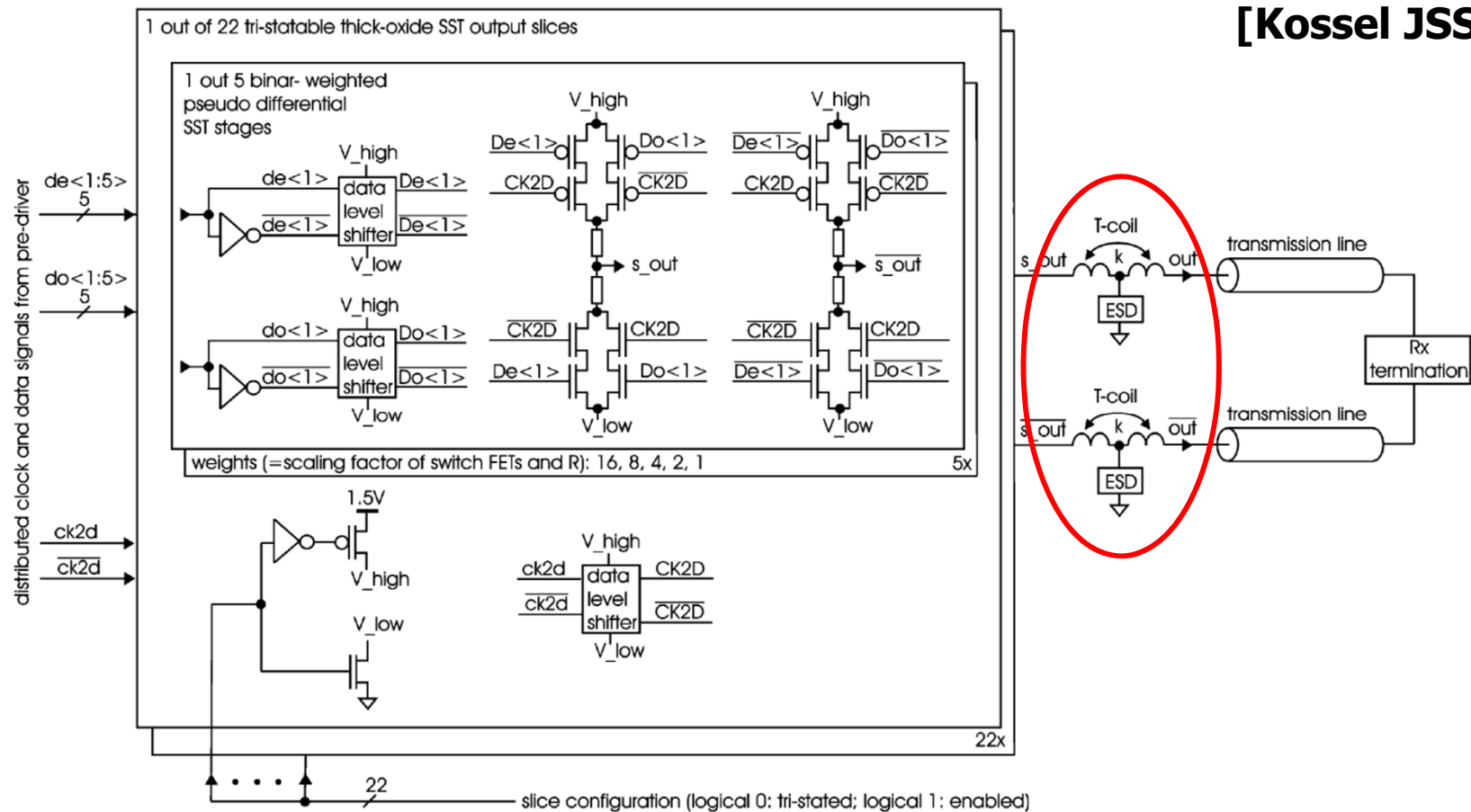
TX Driver Circuits

- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- Swing enhancement techniques
- Impedance control
- Pad bandwidth extension
- Slew-rate control

Output Pad Network Challenges

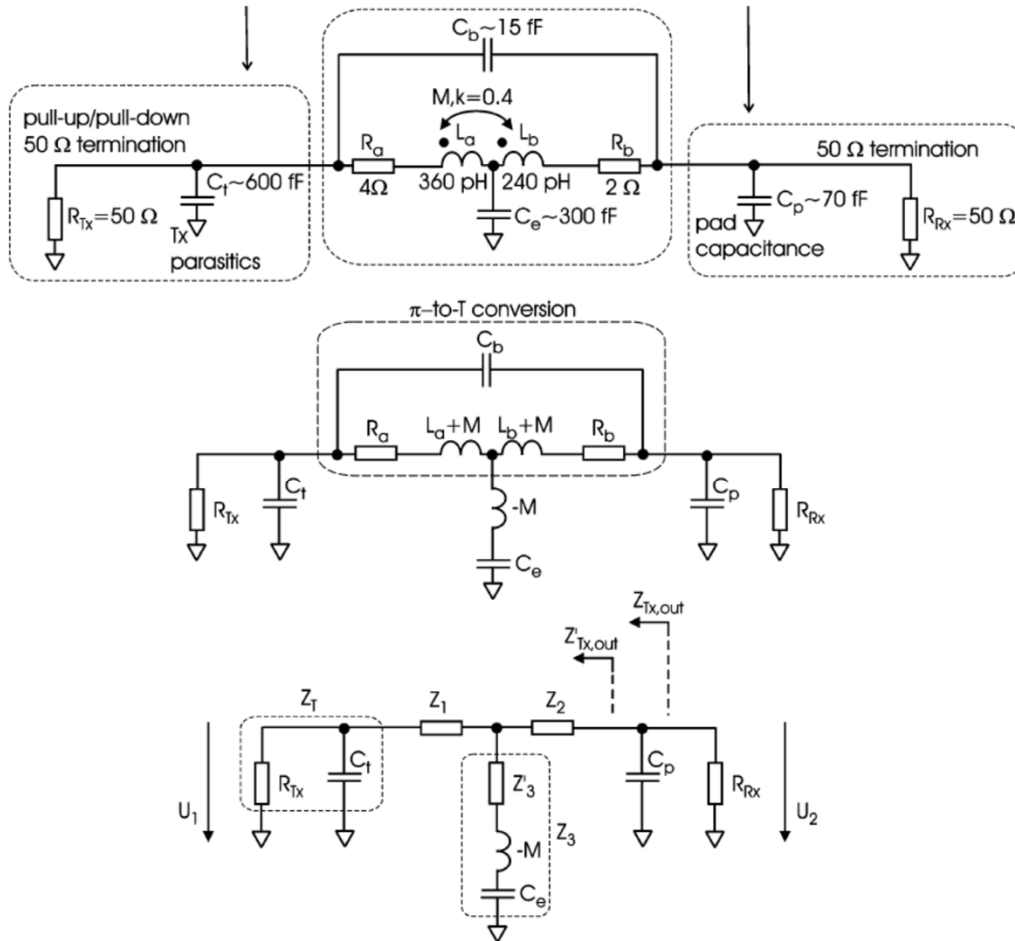
- Meeting return loss (S_{11}) spec
 - $< -7\text{dB}$ at Nyquist
- Maximizing bandwidth with small group delay
- Support ESD
- Balance output network size versus performance

T-Coil Output Stage



- Output T-coil between driver and pad allows for splitting of driver, ESD, and pad capacitance
- Provides significant bandwidth enhancement and improved return loss

T-Coil Equations



[Kossel JSSC 2008]

$$Z'_{Tx,out} = \frac{Z_T \cdot Z_3 + Z_1 \cdot Z_3 + Z_1 \cdot Z_2 + Z_2 \cdot Z_3 + Z_2 \cdot Z_T}{Z_1 + Z_3 + Z_T} \quad (4)$$

$$Z_1 = \frac{(L_a + M) \cdot s + R_a}{D(s)} \quad (5)$$

$$Z_2 = \frac{(L_b + M) \cdot s + R_b}{D(s)} \quad (6)$$

$$Z_3 = \frac{v_4 s^4 + v_3 s^3 + v_2 s^2 + v_1 s + 1}{u_3 s^3 + u_2 s^2 + u_1 s} \quad (7)$$

$$Z_T = \frac{R_{Tx}}{1 + s R_{Tx} C_T} \quad (8)$$

$$Z_{Tx,out} = \frac{Z'_{Tx,out}}{1 + s C_p Z'_{Tx,out}} \quad (9)$$

Output Reflection Factor

$$r = \frac{Z_{Tx,out} - 50 \Omega}{Z_{Tx,out} + 50 \Omega} \quad (10)$$

Parameters: $L_a = 360$ pF, $L_b = 240$ pF, $k = 0.4$, $M = 118$ pF, $C_b = 15$ fF, $C_1 = 600$ fF, $C_p = 70$ fF, $R_{Tx} = R_{Rx} = 50 \Omega$

$$D(s) = C_b(L_a + L_b + 2M) \cdot s^2 + C_b(R_a + R_b) \cdot s + 1$$

$$v_1 = C_b(R_a + R_b) \quad v_2 = R_a R_b C_b C_e + C_b(L_a + L_b + 2M) - M C_e \quad v_3 = C_b C_e(L_a R_b + L_b R_a) \quad v_4 = C_b C_e(L_a L_b - M^2)$$

$$u_1 = C_e \quad u_2 = C_b C_e(R_a + R_b) \quad u_3 = C_b C_e(L_a + L_b + 2M)$$

T-Coil Wiring & Improvement

[Kossel JSSC 2008]

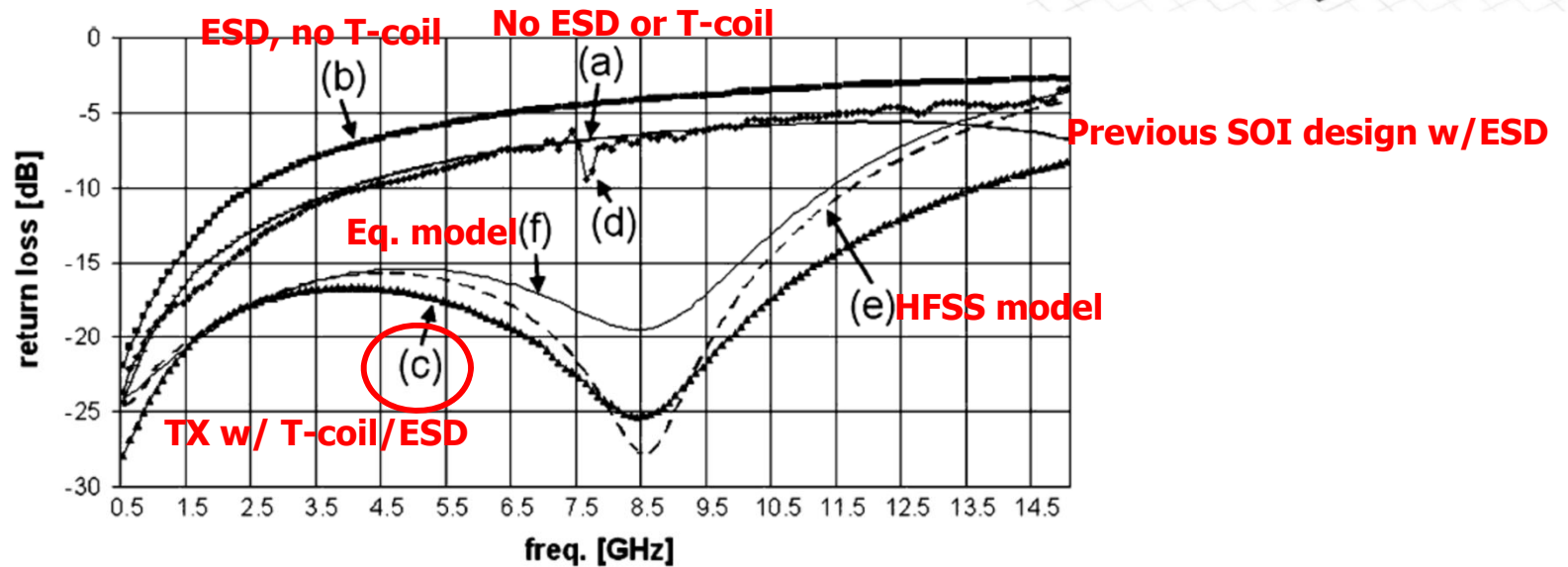
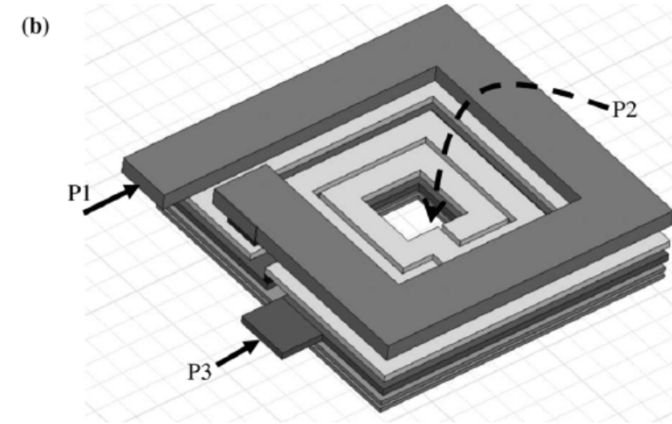
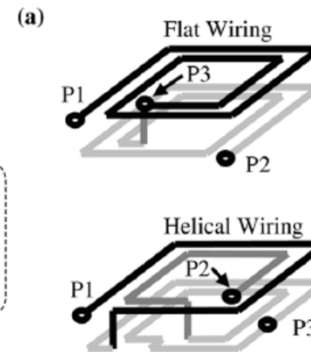
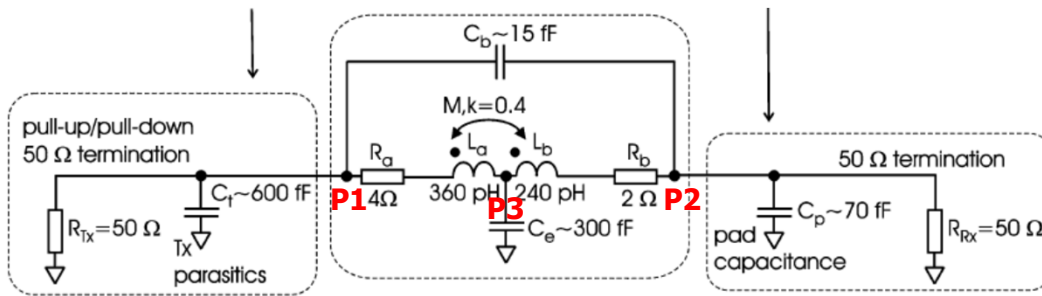
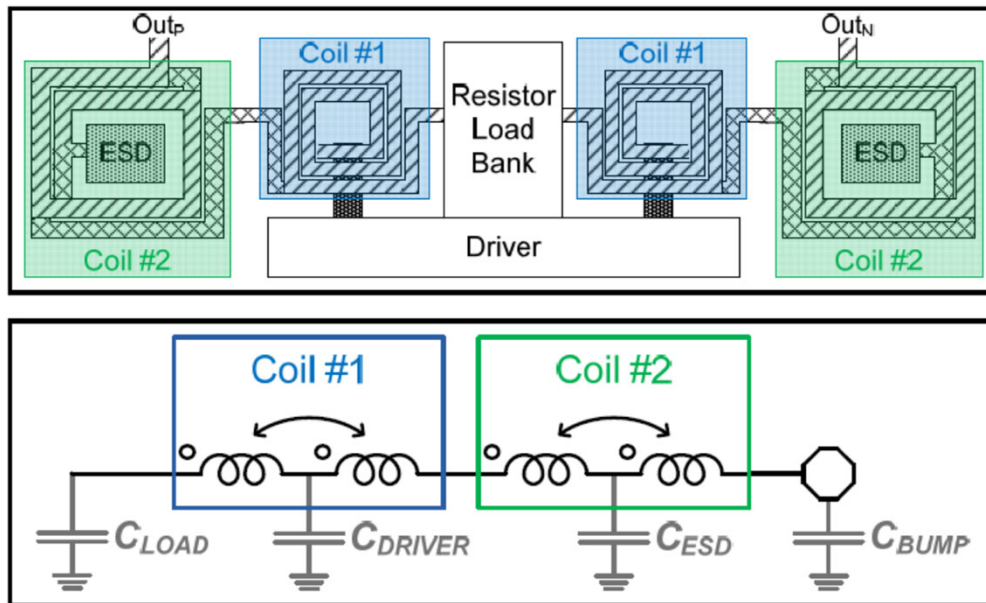


Fig. 22. Measured return loss curves: (a) without ESD and without T-coil; (b) with SCR used as ESD, but no T-coil; (c) with SCR and asymmetric T-coil; (d) SOI CMOS SST transmitter [7] with ESD. Simulated return loss curves: (e) HFSS EM model; (f) mathematical model.

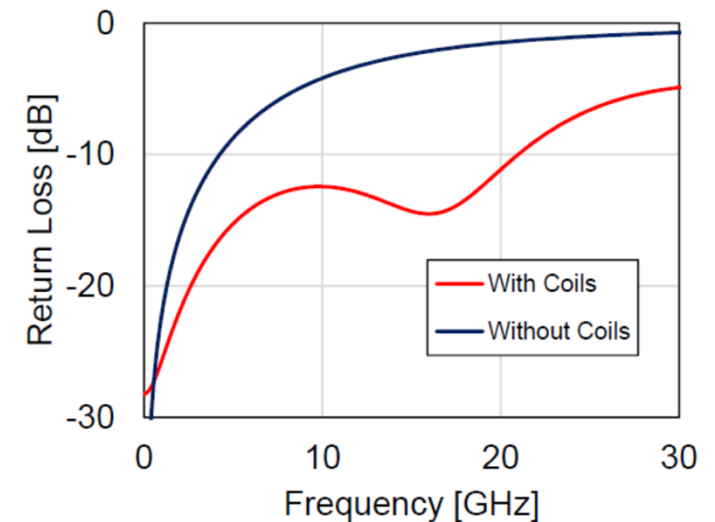
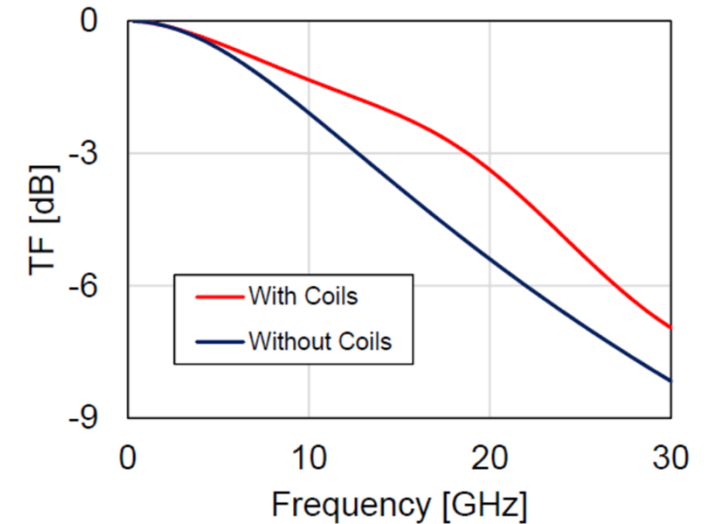
- A helical wiring scheme reduces the vertical parasitic fringing capacitance between layers and improves self-resonance frequency

Double T-Coil Output Bandwidth Extension

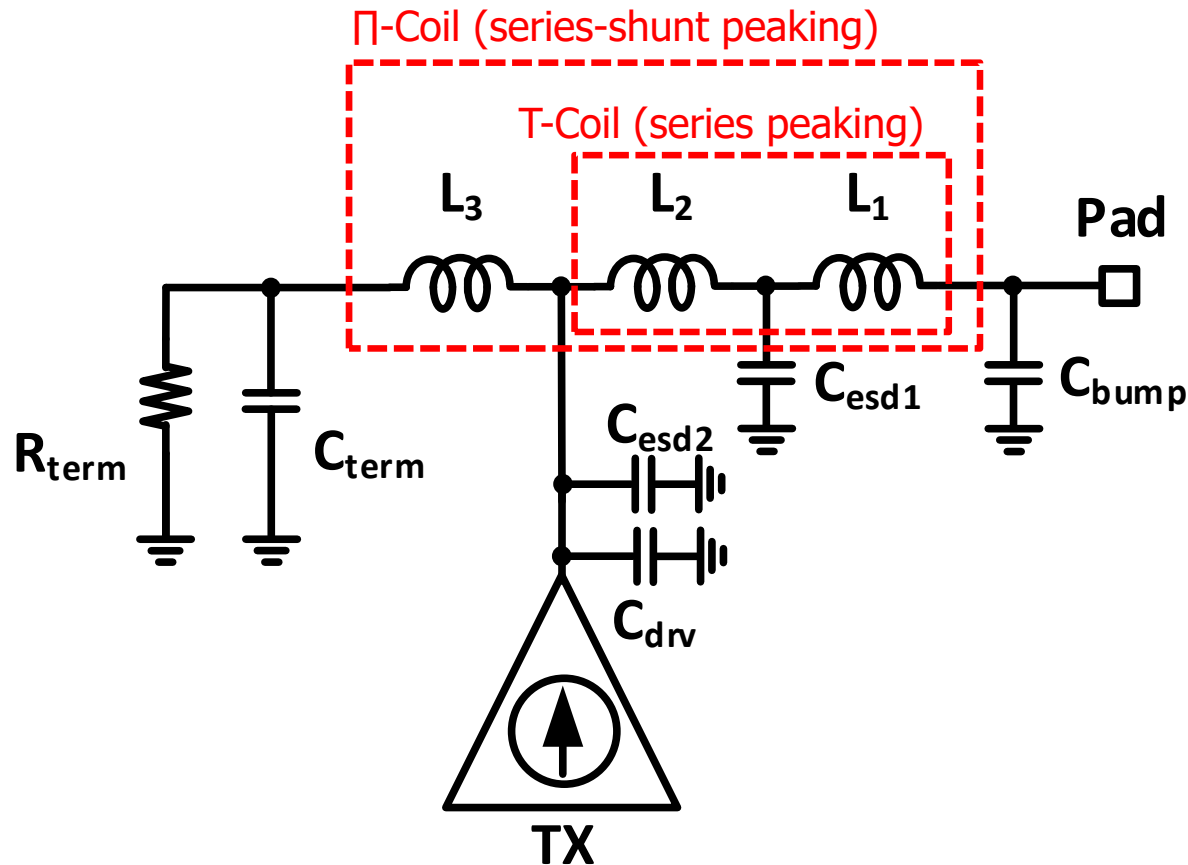


- Double T-coil structure allows separation of termination capacitance
- Enhances bandwidth by 1.5X

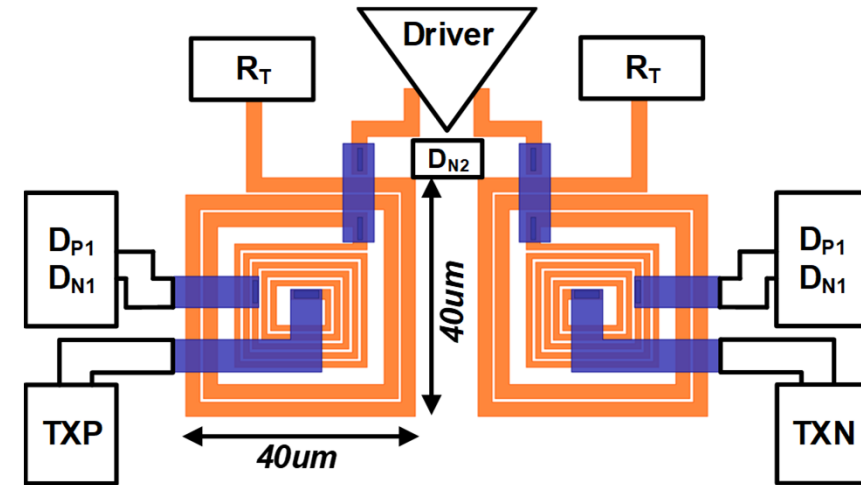
[Steffan ISSCC 2017]



Π -Coil Output Bandwidth Extension



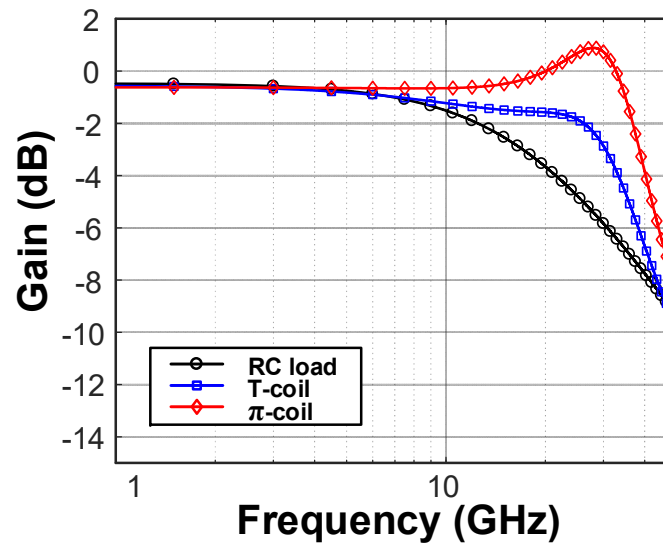
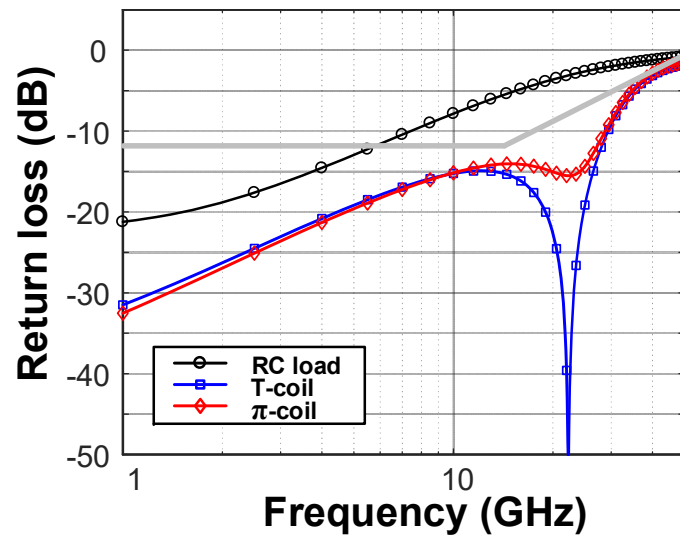
[Kim ISSCC 2019]



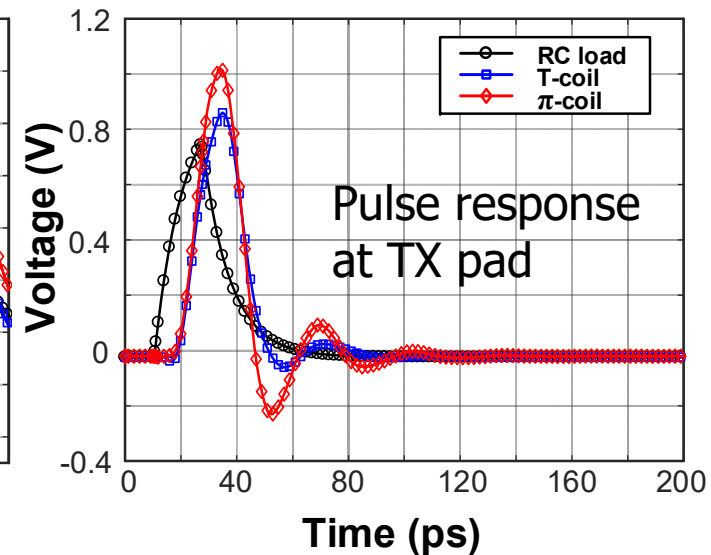
- Output Π -coil provides additional termination capacitance separation
- Provides additional bandwidth extension at the cost of slightly degraded return loss

Π -Coil Output Bandwidth Extension

Response at TX Pad

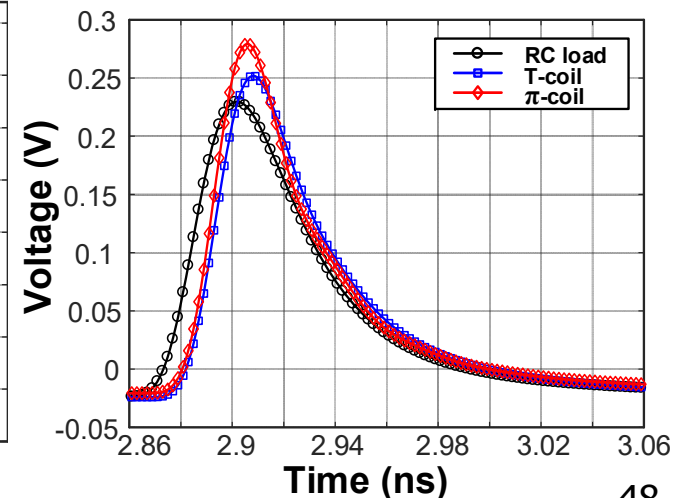
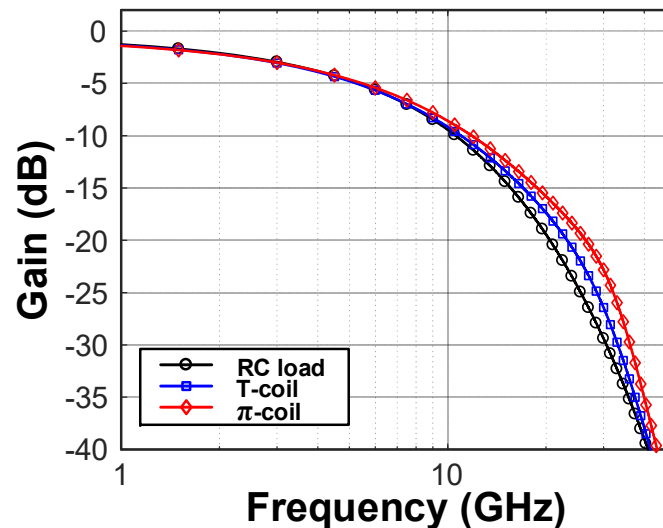


[Kim ISSCC 2019]



- 1-2dB bandwidth peaking results in slightly degraded return loss, but a better pulse response over a low-pass channel

Response after 20dB channel



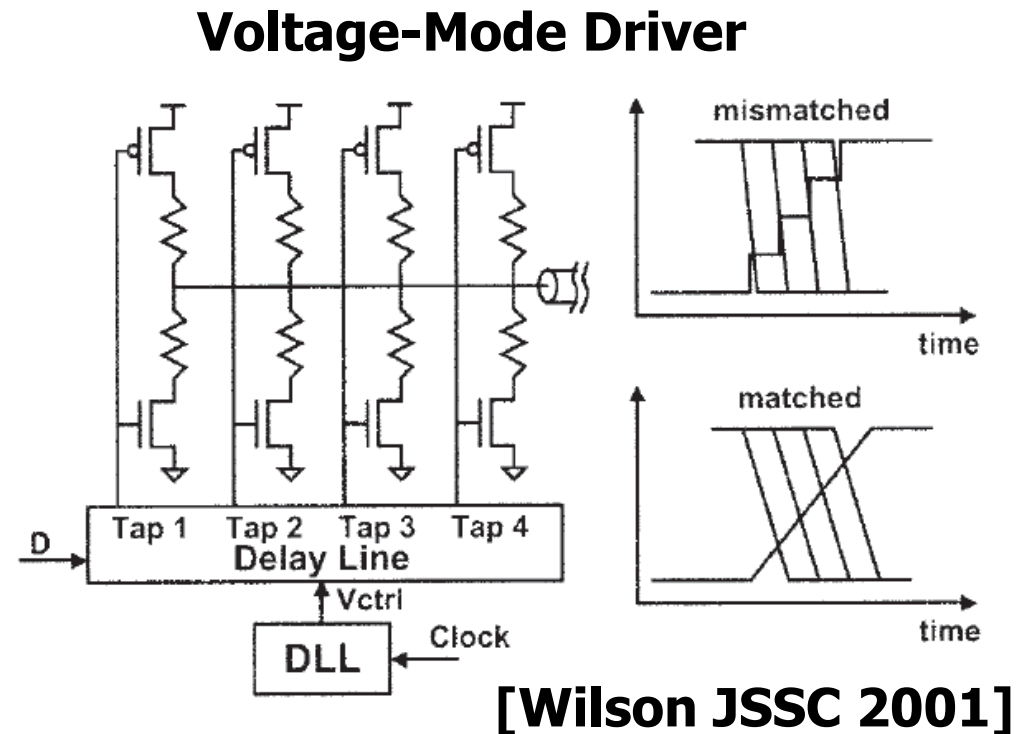
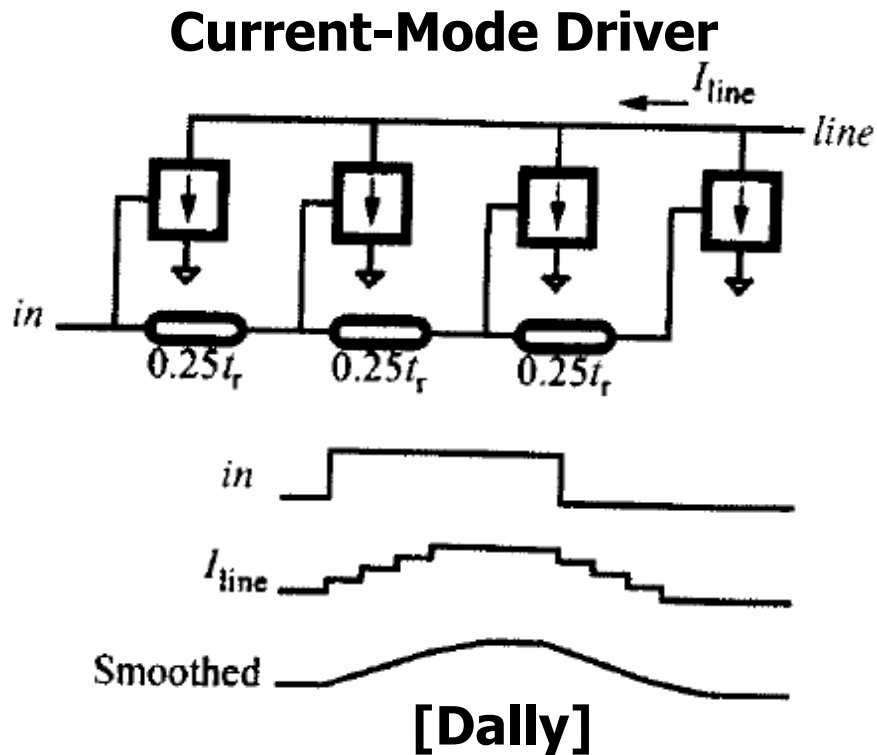
TX Driver Circuits

- Single-ended vs differential signaling
- Controlled-impedance current & voltage-mode drivers
- Swing enhancement techniques
- Impedance control
- Pad bandwidth extension
- Slew-rate control

TX Driver Slew Rate Control

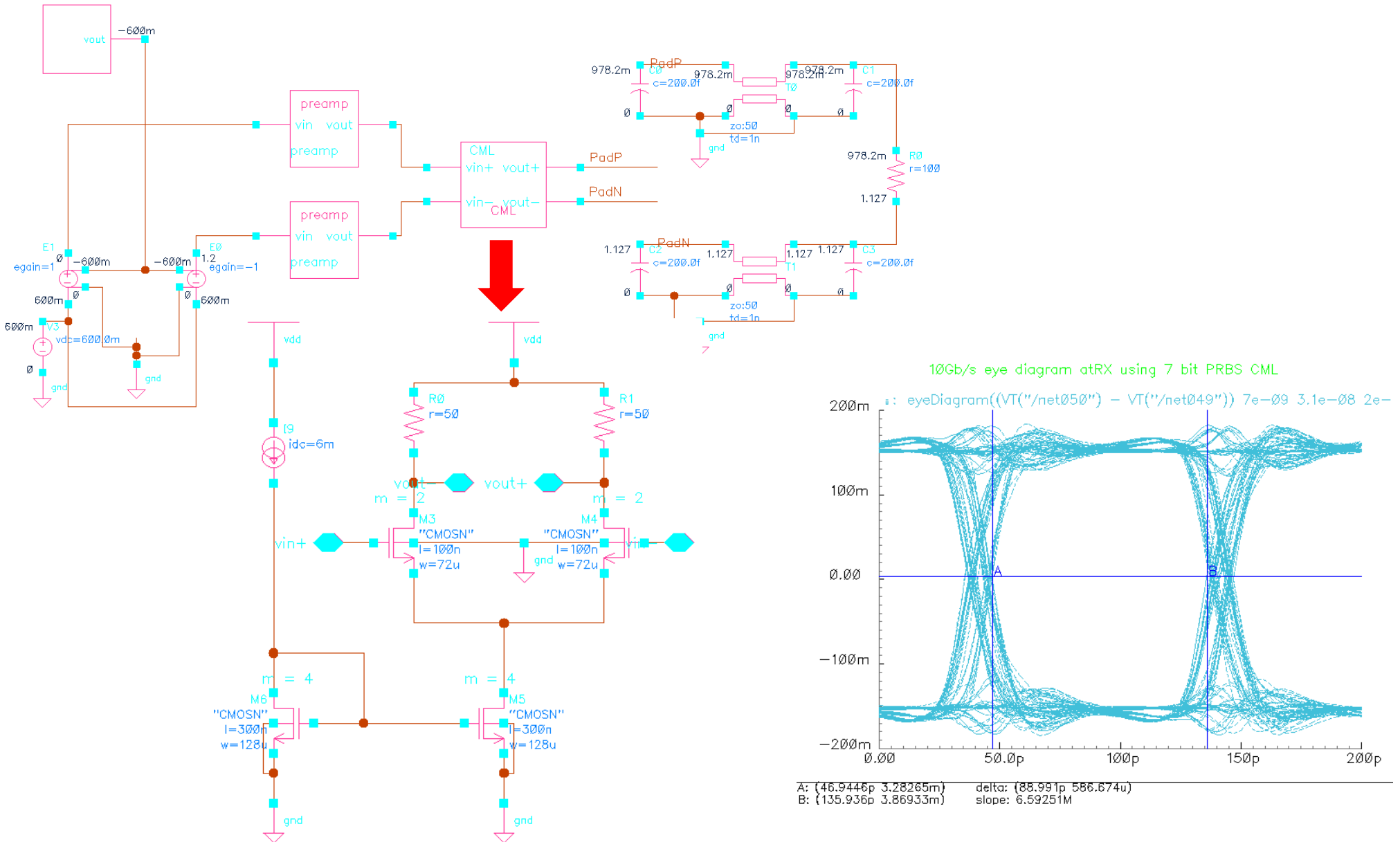
- Output transition times should be controlled
 - Too slow
 - Limits max data rate
 - Too fast
 - Can excite resonant circuits, resulting in ISI due to ringing
 - Cause excessive crosstalk
- Slew rate control reduces reflections and crosstalk

Slew Rate Control w/ Segmented Driver

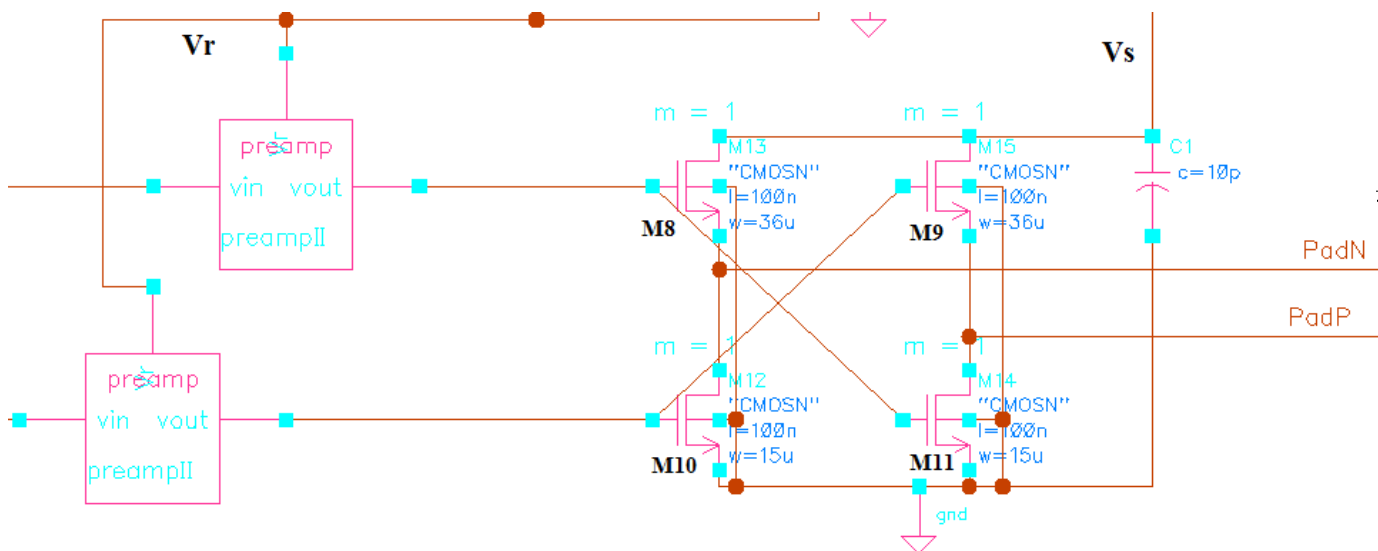
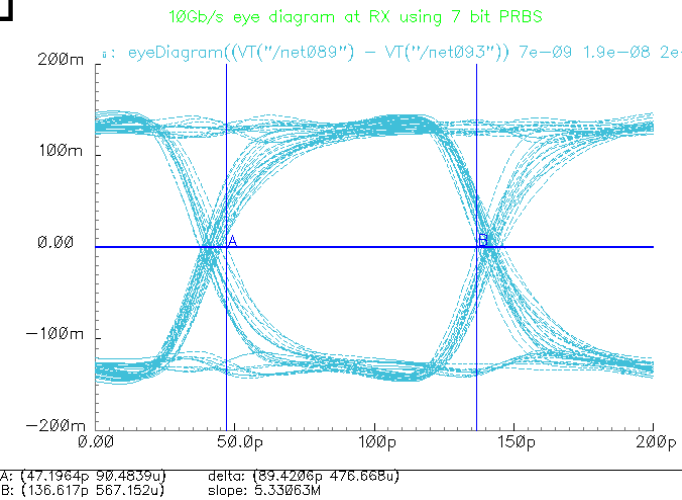
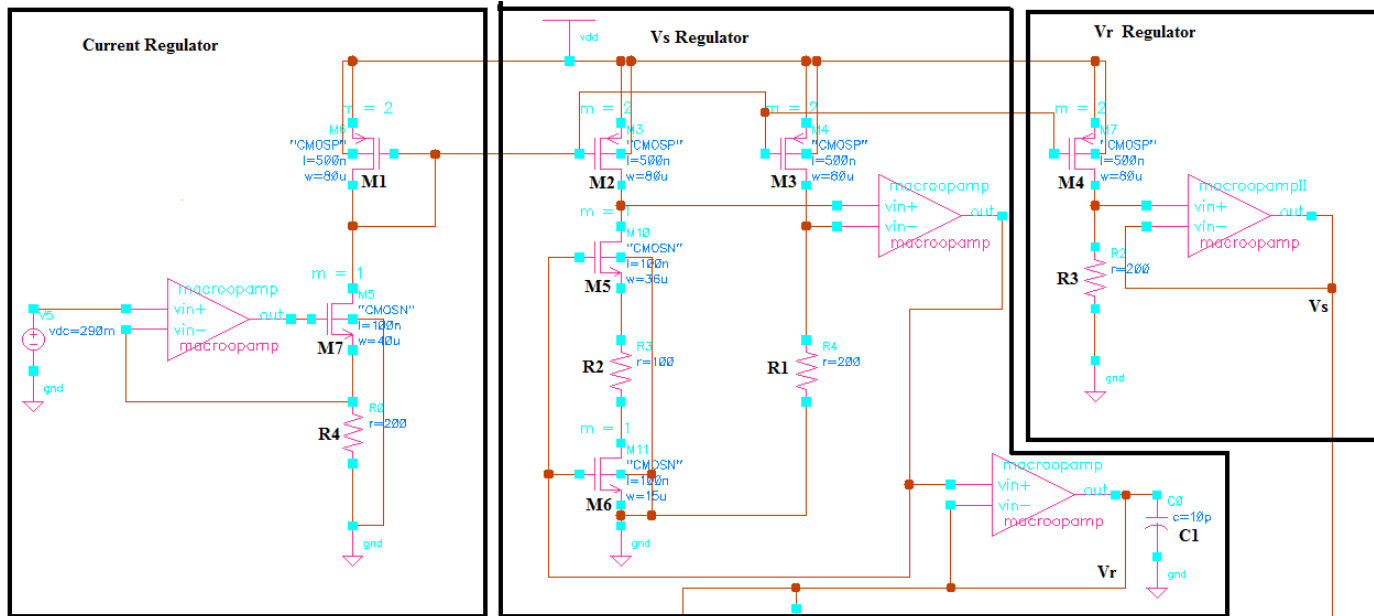


- Slew rate control can be implemented with a segmented output driver
- Segments turn-on time are spaced by $1/n$ of desired transition time
- Pre-driver transition time should also be controlled

Current-Mode Driver Example

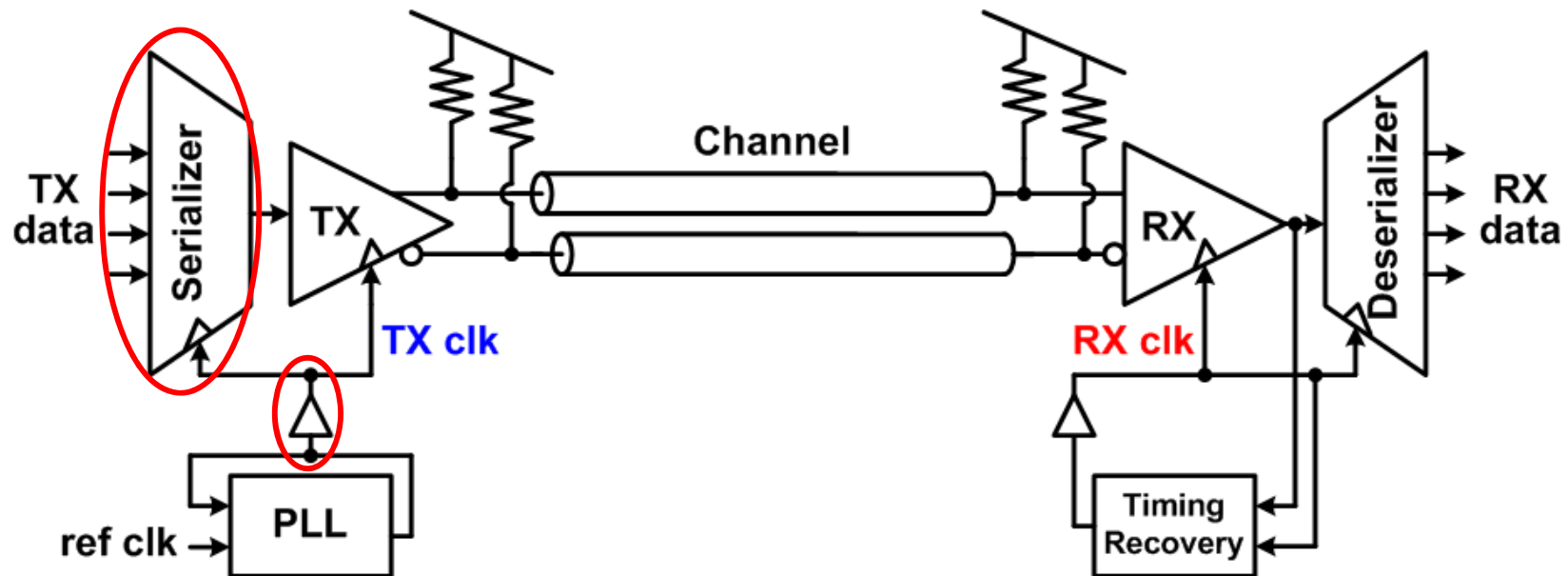


Voltage-Mode Driver Example



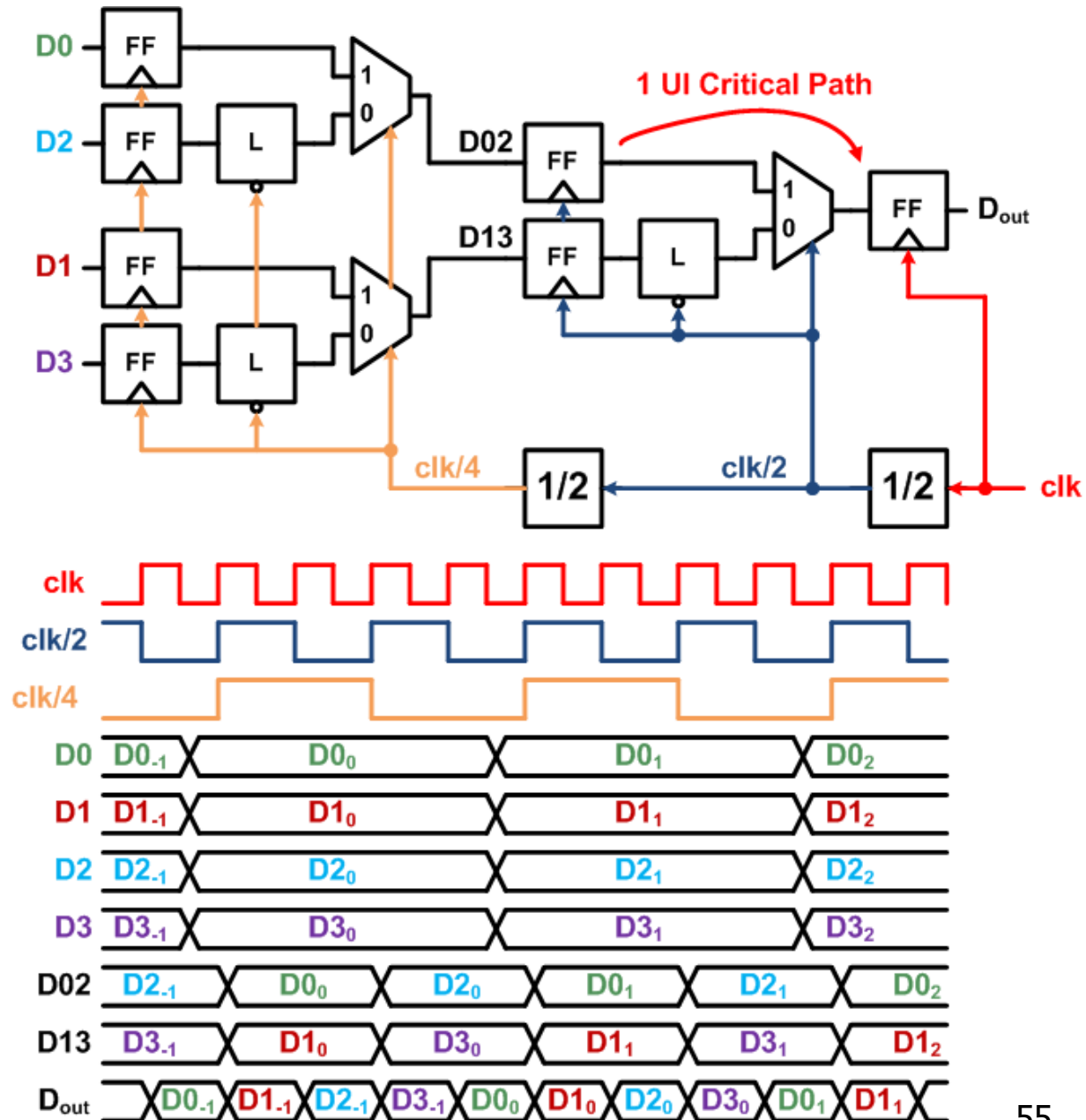
TX Circuit Speed Limitations

- High-speed links can be limited by both the channel and the circuits
- Clock generation and distribution is key circuit bandwidth bottleneck
- Multiplexing circuitry also limits maximum data rate



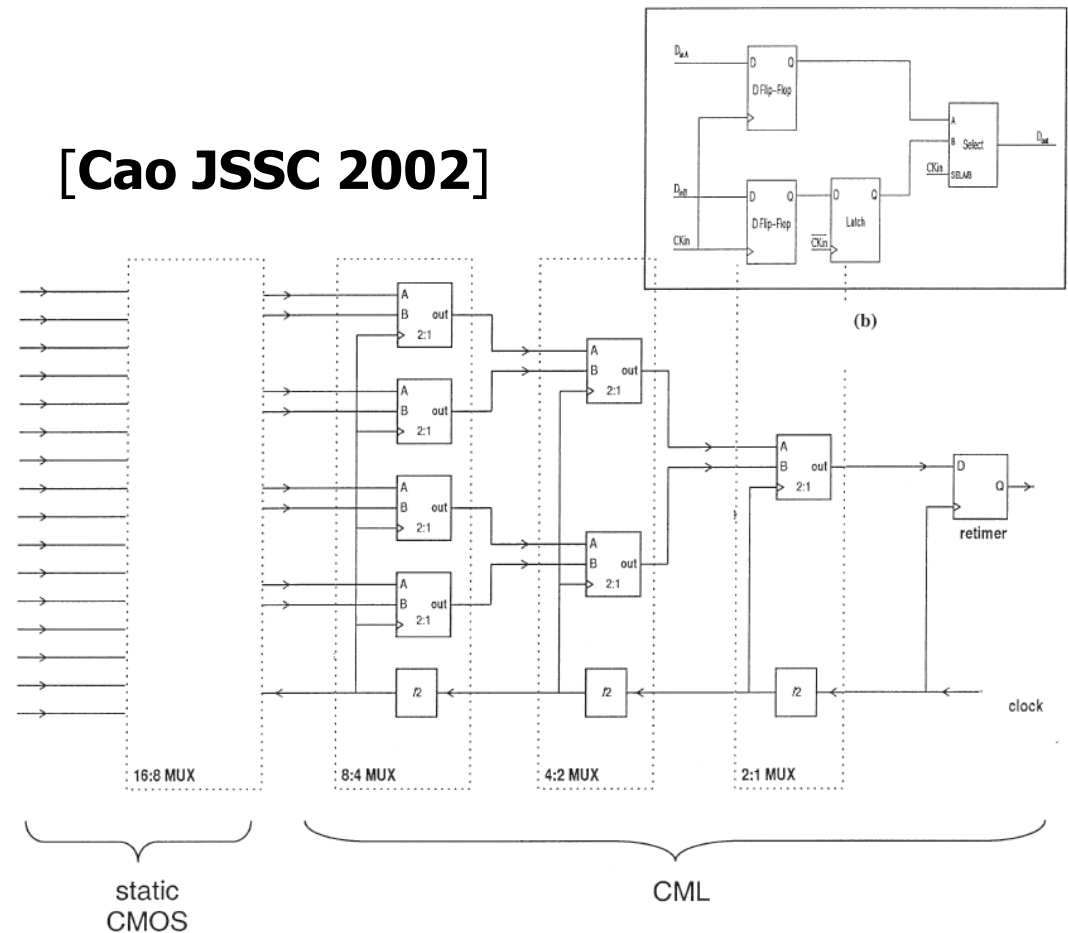
TX Multiplexer – Full Rate

- Tree-mux architecture with cascaded 2:1 stages often used
- Full-rate architecture relaxes clock duty-cycle, but limits max data rate
 - Need to generate and distribute high-speed clock
 - Need to design high-speed flip-flop



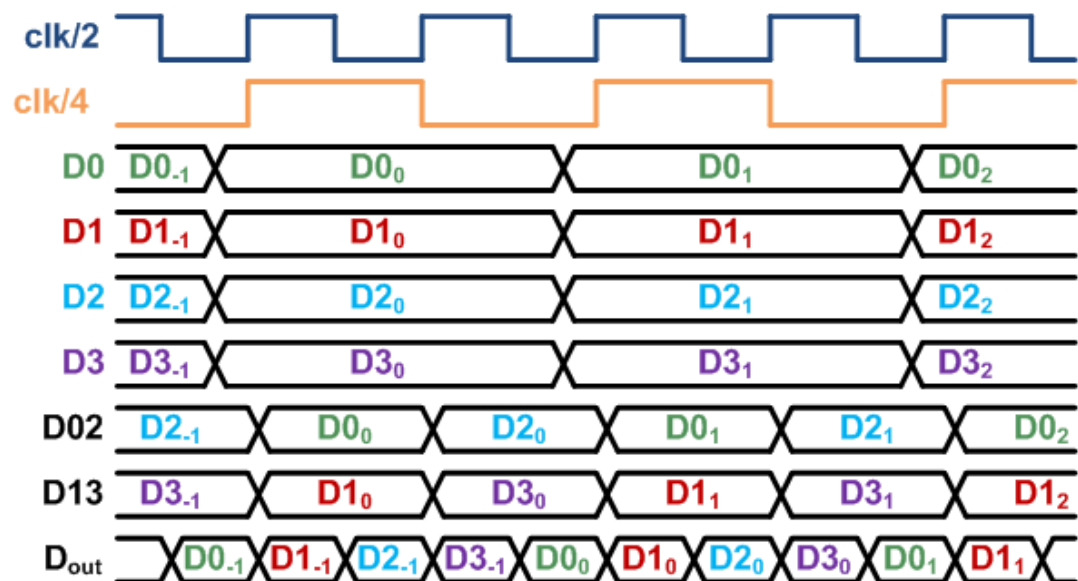
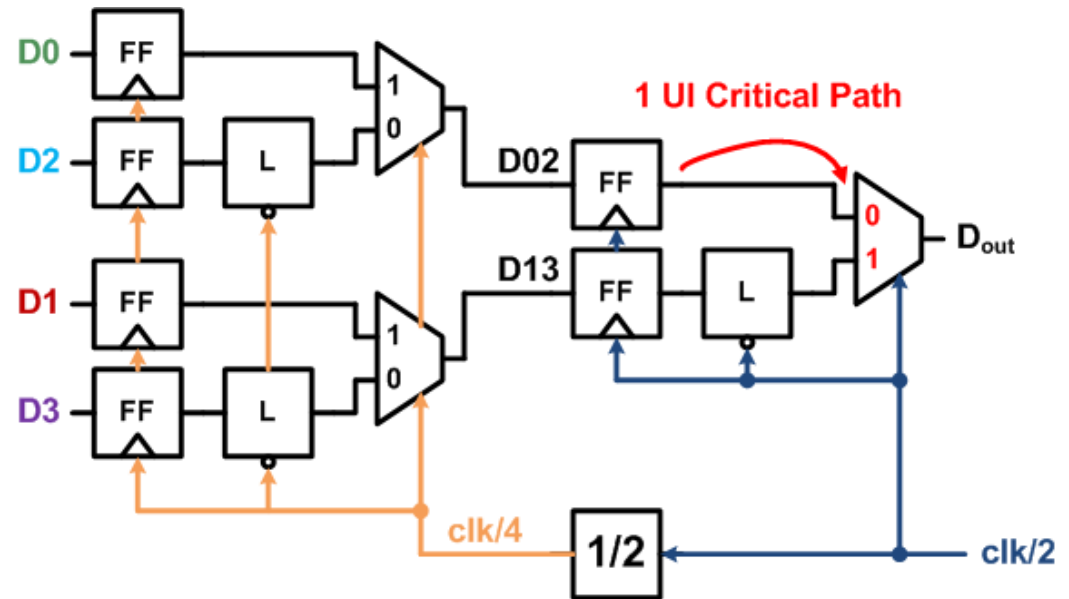
TX Multiplexer – Full Rate Example

- CML logic sometimes used in last stages
 - Minimize CML to save power
- 10Gb/s in 0.18 μ m CMOS
- 130mW!!



TX Multiplexer – Half Rate

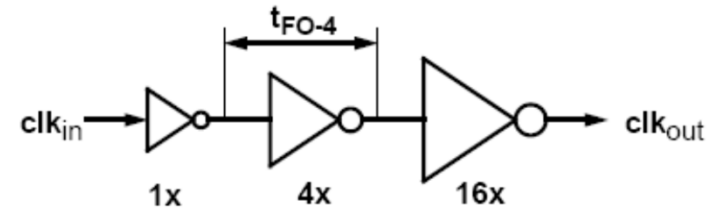
- Half-rate architecture eliminates high-speed clock and flip-flop
- Output eye is sensitive to clock duty cycle
- Critical path no longer has flip-flop setup time
- Final mux control is swapped to prevent output glitches
 - Can also do this in preceding stages for better timing margin



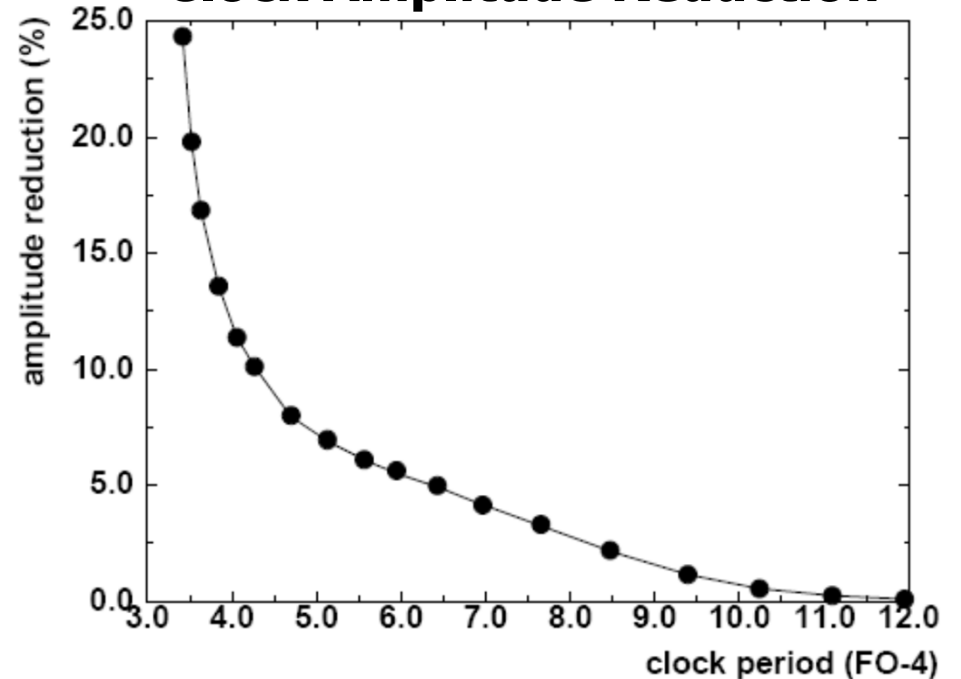
Clock Distribution Speed Limitations

- Max clock frequency that can be efficiently distributed is limited by clock buffers ability to propagate narrow pulses
- CMOS buffers are limited to a min clock period near 8FO4 inverter delays
 - About 4GHz in typical 90nm CMOS
 - Full-rate architecture limited to this data rate in Gb/s
- Need a faster clock → use faster clock buffers
 - CML
 - CML w/ inductive peaking

t_{FO4} in 90nm \sim 30ps



Clock Amplitude Reduction*



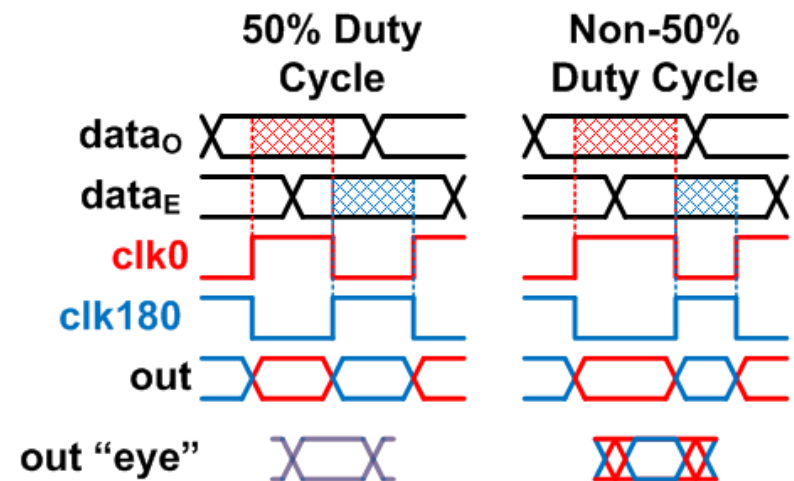
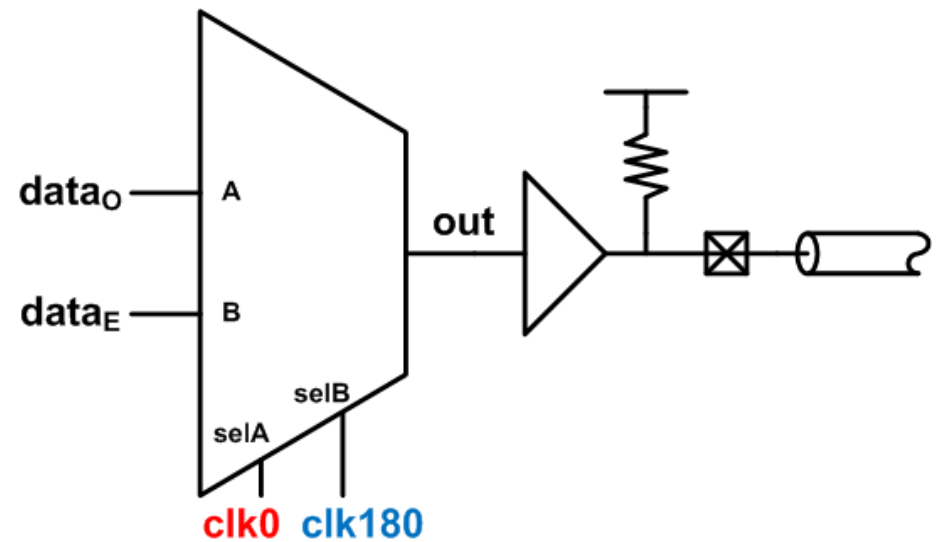
faster

slower

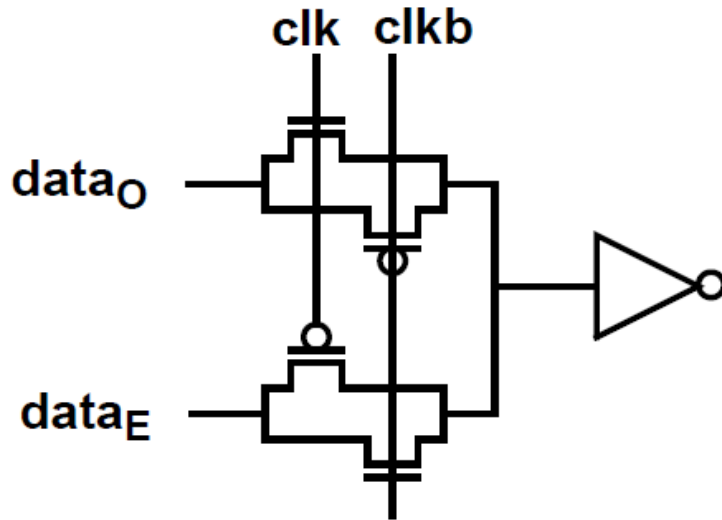
*C.-K. Yang, "Design of High-Speed Serial Links in CMOS," 1998.

Multiplexing Techniques – 1/2 Rate

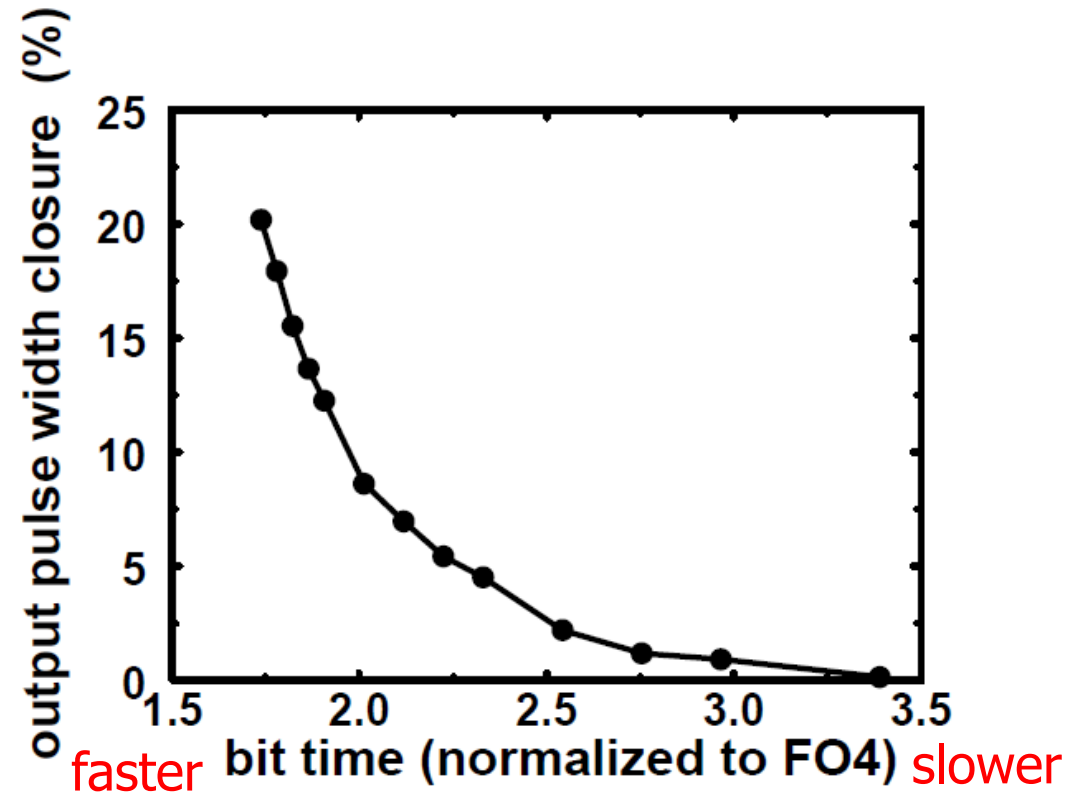
- Full-rate architecture is limited by maximum clock frequency to $8FO4 T_b$
- To increase data rates eliminate final retiming and use multiple phases of a slower clock to mux data
- Half-rate architecture uses 2 clock phases separated by 180° to mux data
 - Allows for $4FO4T_b$
 - 180° phase spacing (duty cycle) critical for uniform output eye



2:1 CMOS Mux

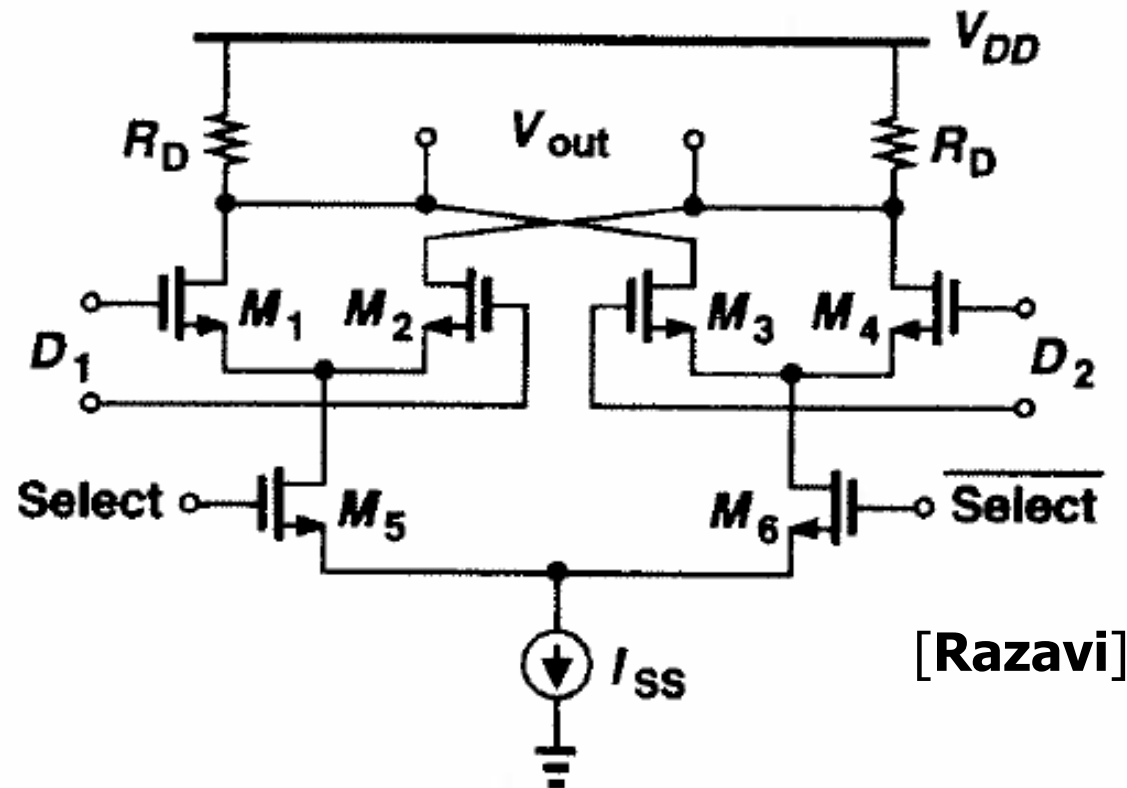


*C.-K. Yang, "Design of High-Speed Serial Links in CMOS," 1998.



- 2:1 CMOS mux able to propagate a minimum pulse near $2FO4 T_b$
- However, with a $\frac{1}{2}$ -rate architecture still limited by clock distribution to $4FO4 T_b$
 - 8Gb/s in typical 90nm

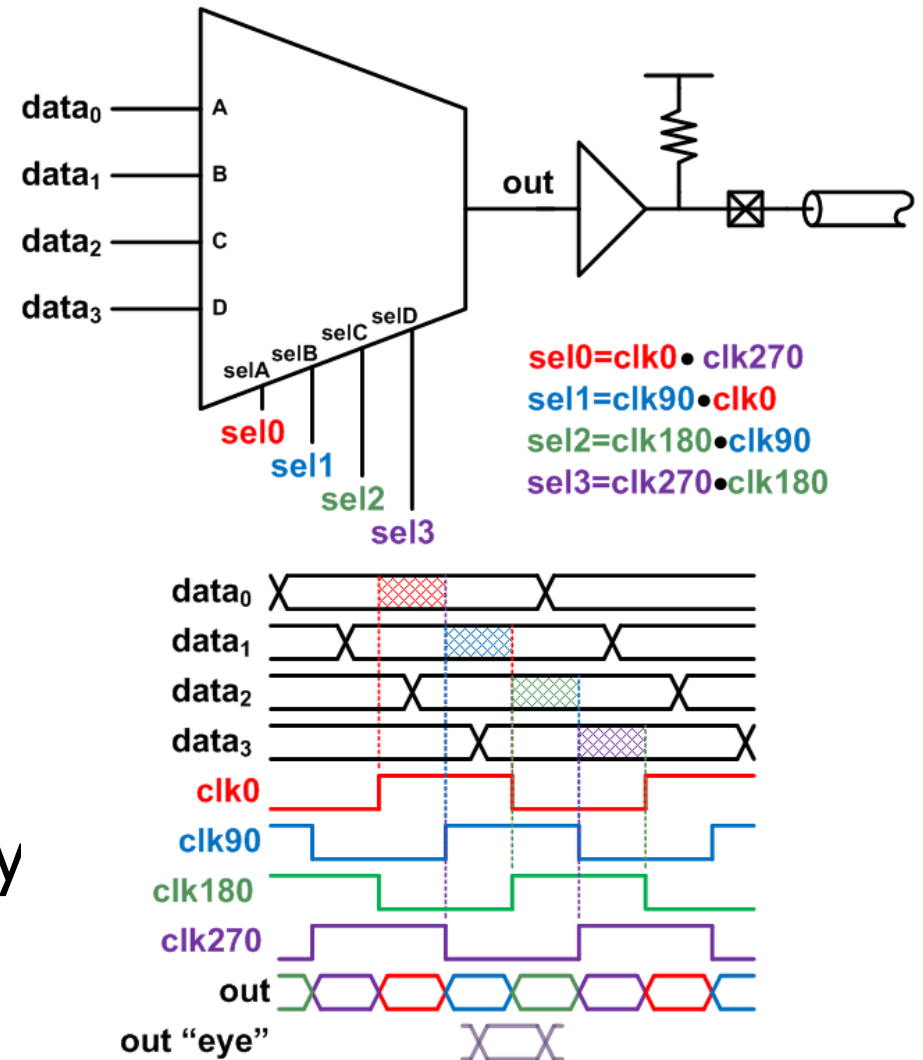
2:1 CML Mux



- CML mux can achieve higher speeds due to reduced self-loading factor
 - Cost is higher power consumption that is independent of data rate (static current)

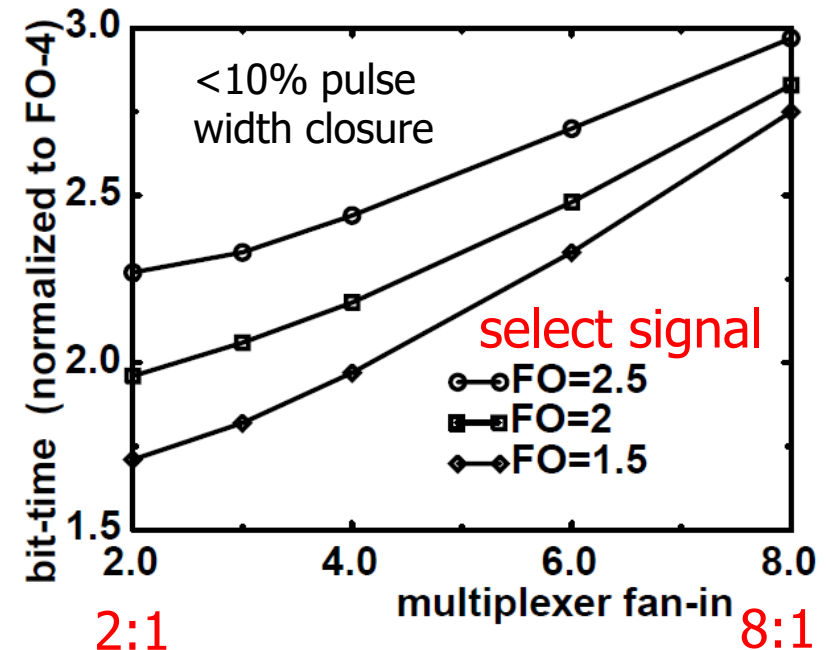
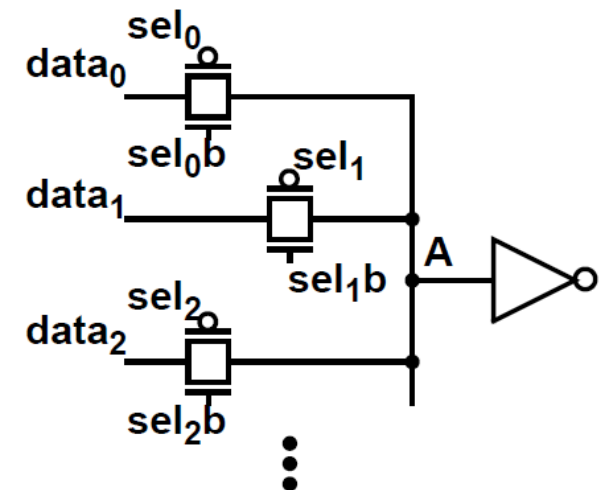
Increasing Multiplexing Factor – 1/4 Rate

- Increase multiplexing factor to allow for lower frequency clock distribution
- 1/4-rate architecture
 - 4-phase clock distribution spaced at 90° allows for 2FO4 Tb
 - 90° phase spacing and duty cycle critical for uniform output eye

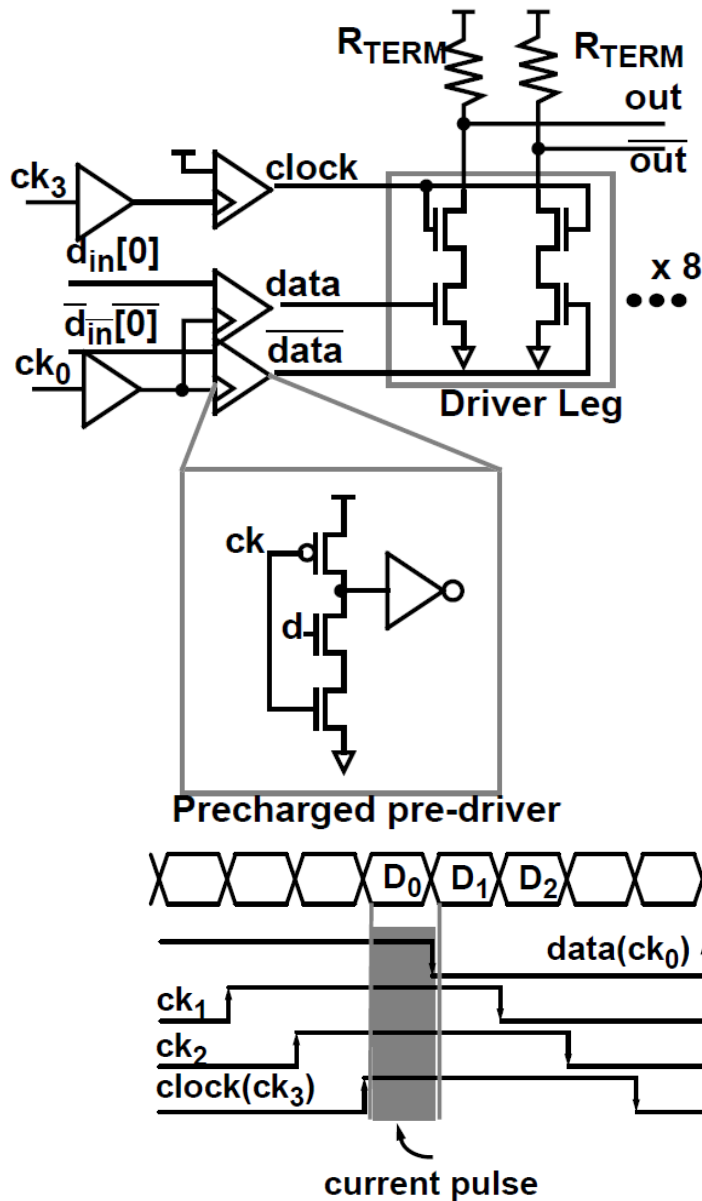


Increasing Multiplexing Factor – Mux Speed

- Higher fan-in muxes run slower due to increased cap at mux node
- 1/4-rate architecture
 - 4:1 CMOS mux can potentially achieve $2FO_4 T_b$ with low fanout
 - An aggressive CMOS-style design has potential for 16Gb/s in typical 90nm CMOS
- 1/8-rate architecture
 - 8-phase clock distribution spaced at 45° allows for $1FO_4 T_b$
 - No way a CMOS mux can achieve this!!

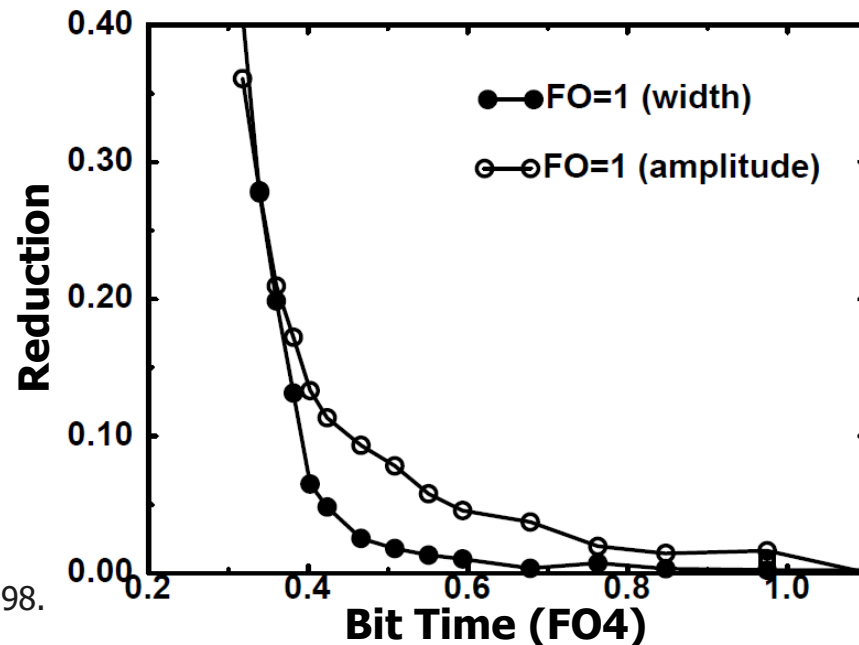


High-Order Current-Mode Output-Multiplexed



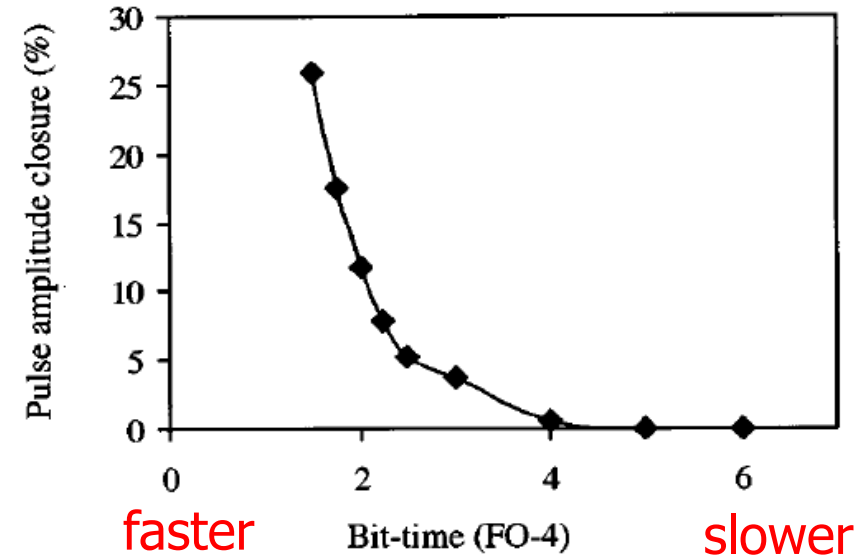
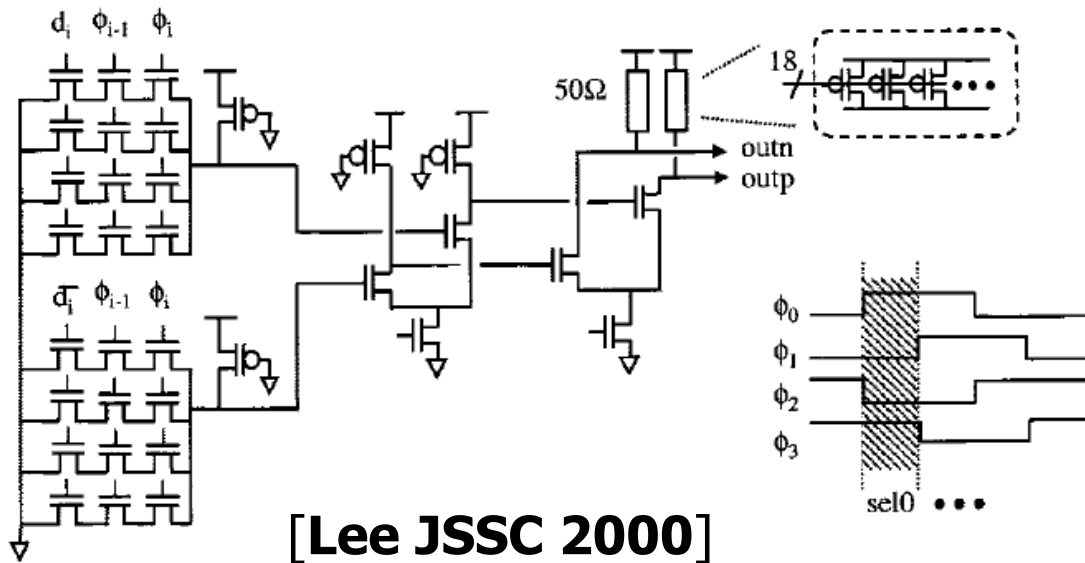
- 8:1 current-mode mux directly at output pad
- Makes sense if output time constant smaller than on-chip time constant

$$\tau_{out} = 25\Omega \times C_{out}$$
- Very sensitive to clock phase spacing
- Yang achieved 6Gb/s in 0.35 μ m CMOS
 - Equivalent to 33Gb/s in 90nm CMOS (now channel (not circuit) limited)



*C.-K. Yang, "Design of High-Speed Serial Links in CMOS," 1998.

Current-Mode Input-Multiplexed



- Reduces output capacitance relative to output-multiplexed driver
 - Easier to implement TX equalization
- Not sensitive to output stage current mismatches
- Reduces power due to each mux stage not having to be sized to deliver full output current

Next Time

- Receiver Circuits
 - RX parameters
 - RX static amplifiers
 - Clocked comparators
 - Circuits
 - Characterization techniques
 - Integrating receivers
 - RX sensitivity
 - Offset correction