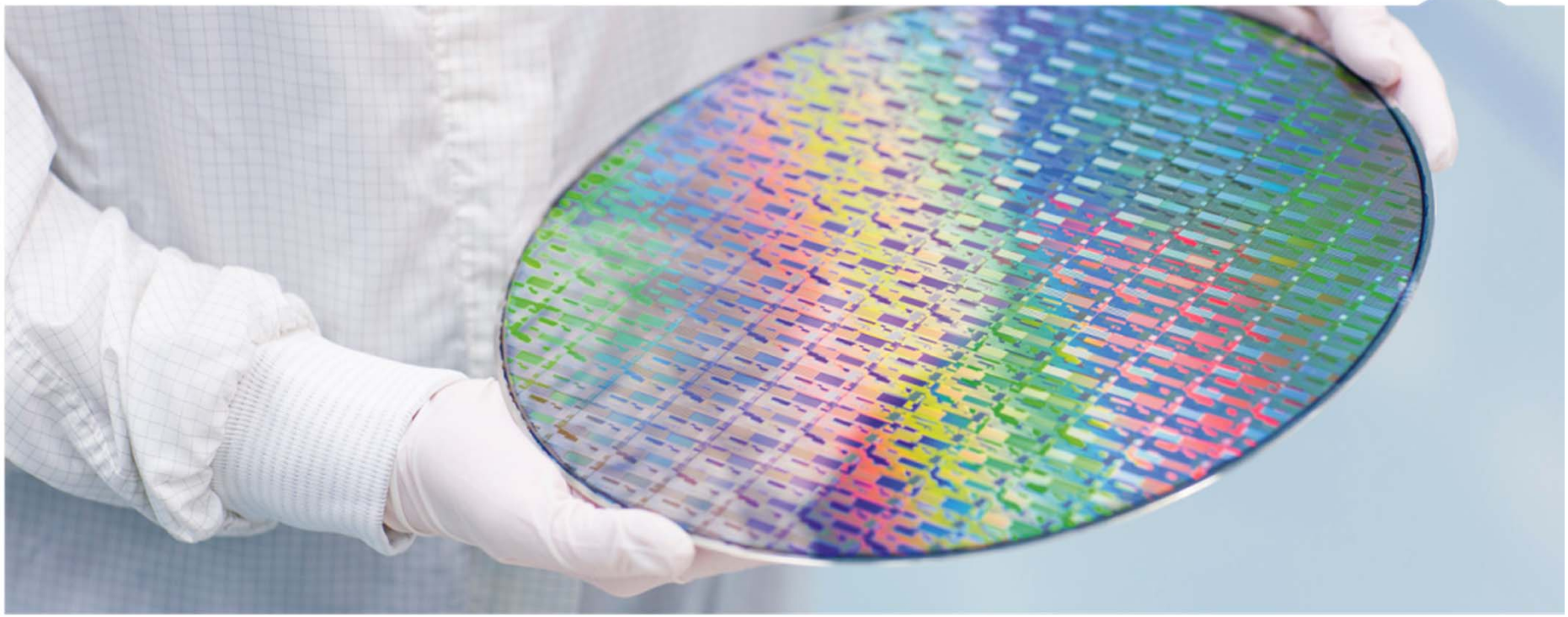
DRIVE INNOVATION · DELIVER EXCELLENCE >

ASM



ENABLING ADVANCED WAFER PROCESSING WITH NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 11, 2017

CAUTIONARY NOTE

Cautionary Note Regarding Forward-Looking Statements: All matters discussed in this presentation, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholders or other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's reports and financial statements. The Company assumes no obligation nor intends to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **New Materials and 3D: Moore's law enablers**
  - ASM technology focus: enabling new materials and new device integration roadmaps
  - Logic scaling
- **ALD**
  - Key strengths of the technology
  - Selected applications in 3D-NAND, DRAM, logic and Emerging Memory
- **PECVD**
- **Vertical Furnace**
- **Epitaxy – Introducing Intrepid® ES™**
  - Epi technology trends
  - Intrepid ES features & benefits

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  - Intrepid ES features & benefits

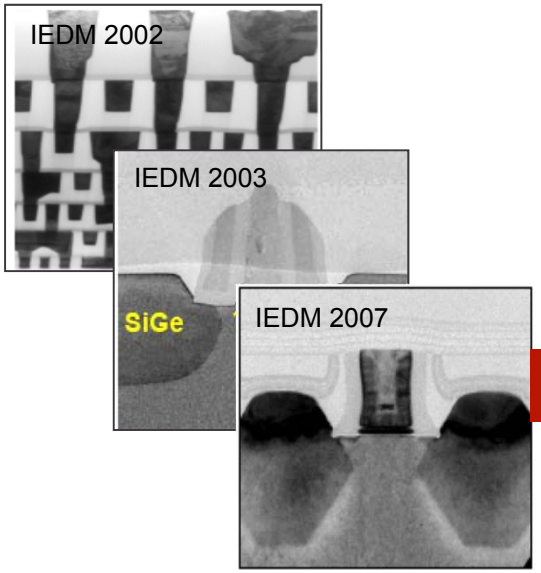
MOORE'S LAW IS INCREASINGLY ENABLED BY NEW MATERIALS AND 3D TECHNOLOGIES

1990 1995 2000 2005 2010 2015 2020 2025

Scaling enabled by Litho

Patterning Spacers

Multi-Color ESL Self-aligned



Scaling enabled by Materials

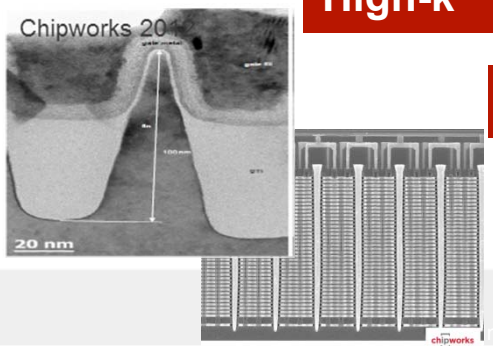
Low-k

Strained Si

High-k

High-mobility Materials

Scaling enabled by 3D



FinFET

3D TSV

CFET

3D Memory

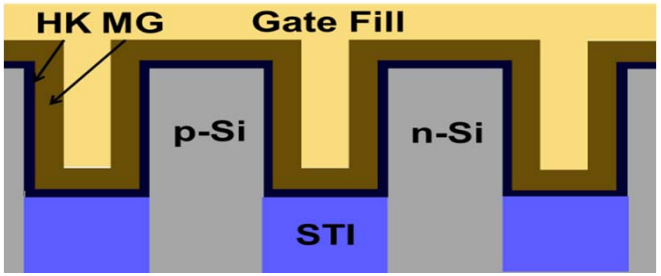
HGAA

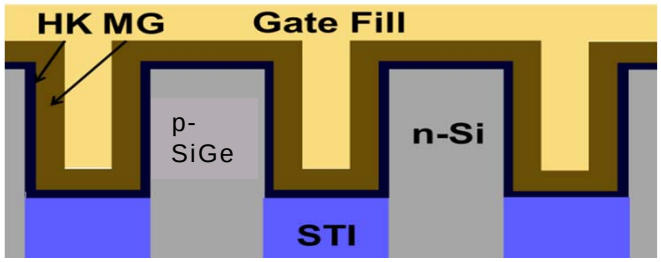
3D CMOS

LOGIC SCALING BY MATERIALS AND 3D

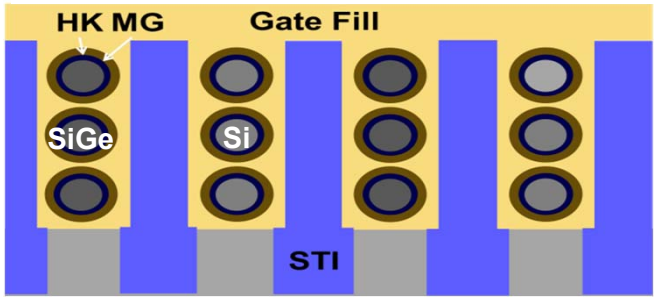
2011

FinFET Device





Next Device Architecture – Horizontal/Vertical GAA



~2023

- **Density scaling (continuing Moore's law) driving towards higher mobility, lower resistivity and very conformal materials**
- **Future systems will integrate much wider variety of materials and device architectures**

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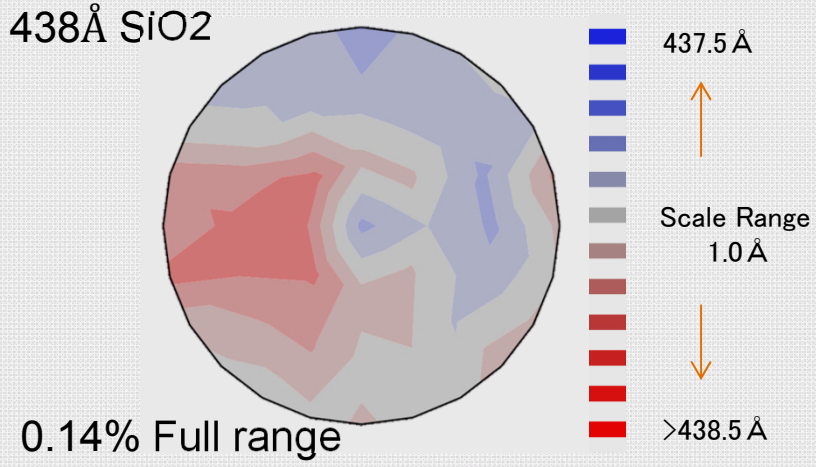
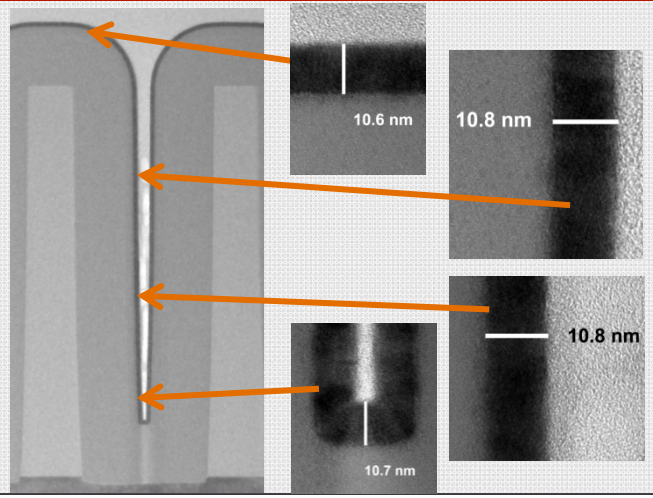
ALD - ENABLER OF NEW MATERIALS - KEY STRENGTHS OF ALD

Uniformity



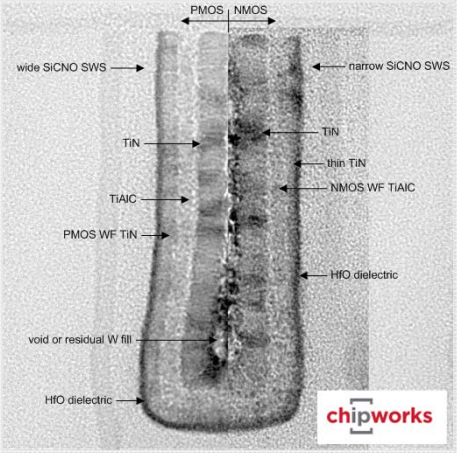
Step Coverage



108Å TiN

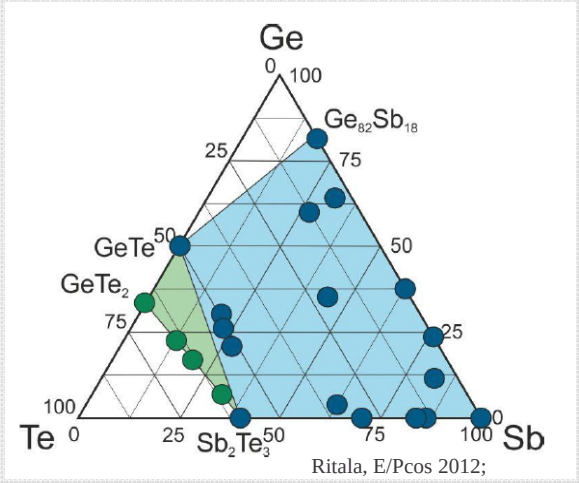
98% step coverage

Interface Control



Atomically engineered interfaces to optimize leakage current, reliability and work-functions

Composition Control



Ritala, E/Pcos 2012;

Excellent composition control for ternary alloys; all ALD solution demonstrated for GST

DEPLOYING THE ADVANTAGES OF ALD

	HAR (>10) Step Coverage	Interface Control	Composition Control	Uniformity	Low Temperature
DRAM Capacitor	✓	✓	✓	✓	
e-DRAM (FEOL)	✓	✓	✓	✓	
High-k / Metal Gate Stack		✓	✓	✓	
e-DRAM (BEOL)	✓	✓	✓	✓	✓
Double Patterning			✓	✓	✓
Liners and Spacers		✓	✓	✓	✓
3D-NAND and Emerging Mem.	✓	✓	✓	✓	✓

ASM PRODUCTS
ALD

› Pulsar® XP

- ALD Hf based high-k gate dielectrics
- ALD metal oxides for etch stops, liners and pattern assist layers
- Cross-flow reactor
- Solid source delivery system

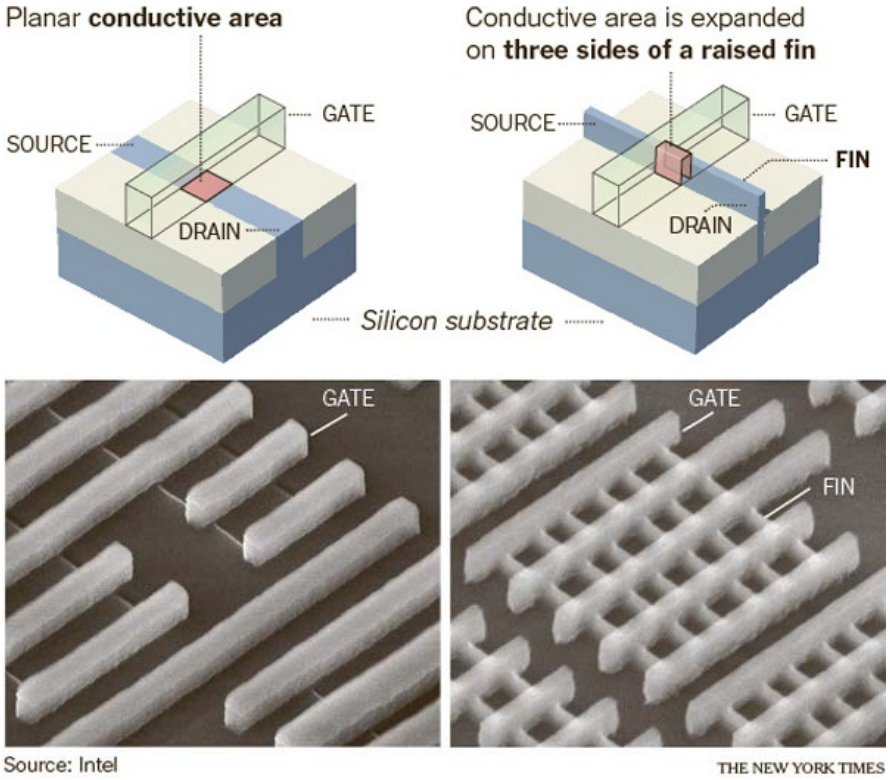
Pulsar® XP

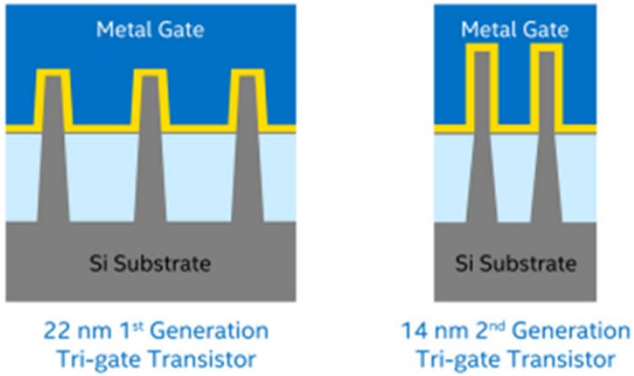
› EmerALD® XP

- ALD metal gate electrodes
- ALD metal nitrides for capacitor electrodes
- Showerhead reactor

EmerALD® XP

FINFET CHALLENGES:
ALD ENABLES FURTHER SCALING IN 3D



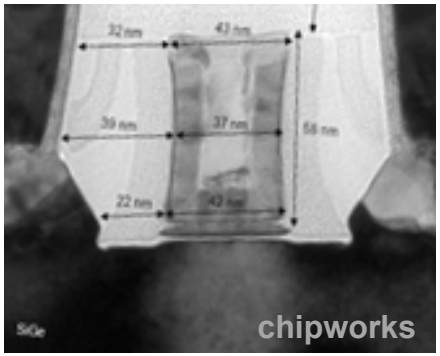


	22nm node	14nm node	10nm node
Fin pitch [nm]	60	42	34
Gate pitch [nm]	90	70	54
Metal pitch [nm]	80	52	36

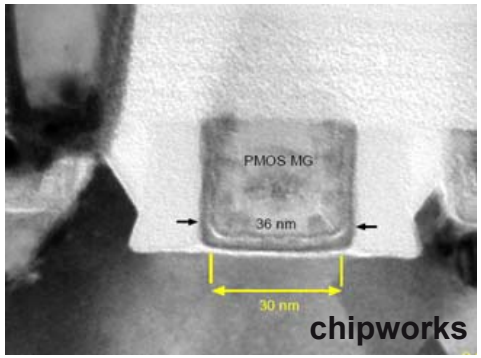
Source: Intel

- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- Aspect ratios increase going from 22nm to 14nm to 10nm
- → ALD technology remains critical for HK and MG layers

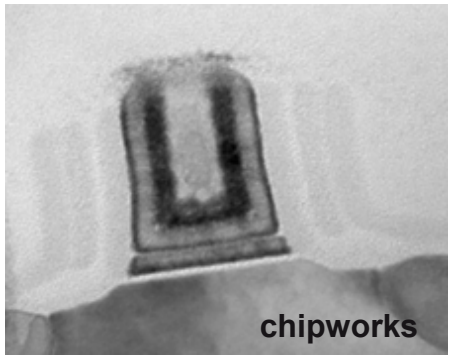
EXTENDIBILITY OF HAFNIUM BASED OXIDES



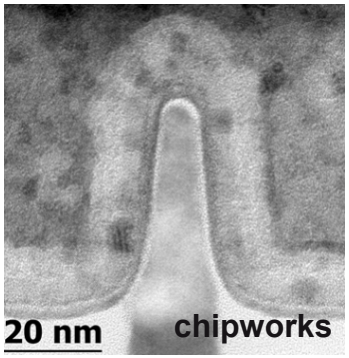
45nm HK first RPMG
Planar FET



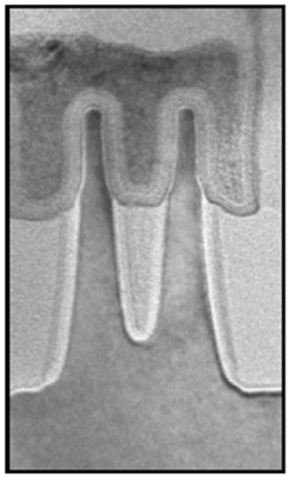
32 nm HK last RPMG
Planar FET

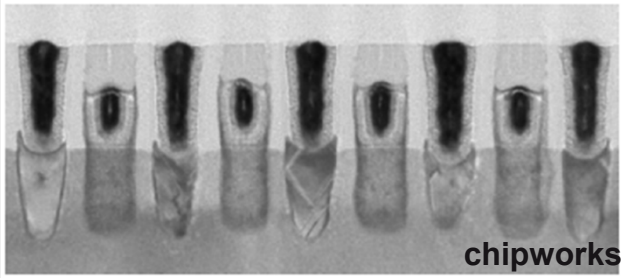


28nm HK first RPMG
Planar FET

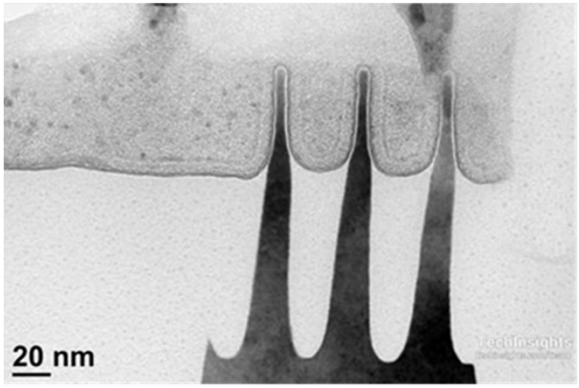


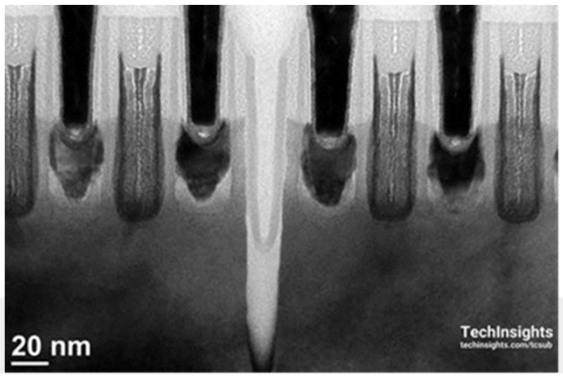
22nm HK last RPMG
FinFET





14nm HK last RPMG
FinFET

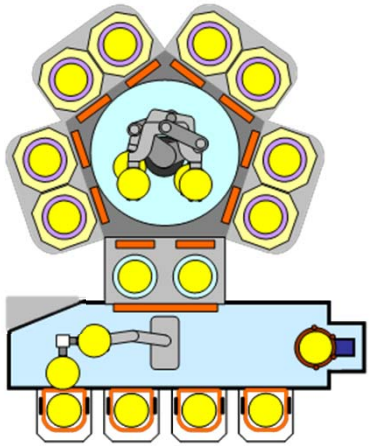




10nm HK last
RPMG
FinFET plus
additional HK
tuning layer

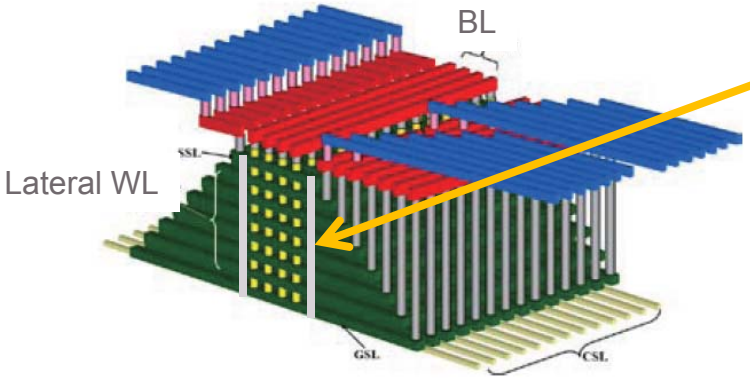
XP8-DCM

- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers by DCM
- PEALD and PECVD can be integrated on the same platform



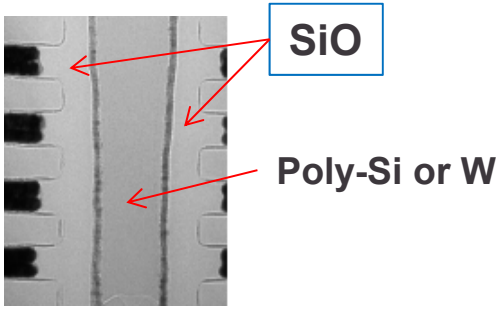
DCM (Dual Chamber Module)

ALD FOR 3D-NAND APPLICATIONS

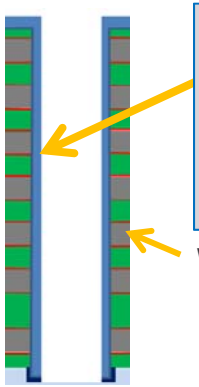


Samsung VLSI Symp 2009

(1) Source contact/Separation slit



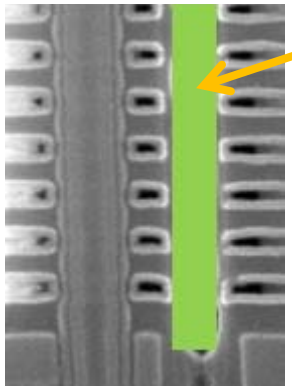
(1-1) High quality PEALD SiO for slit sidewall protection of source contact



Low temperature & high quality SiO without damaging WL metal

WL

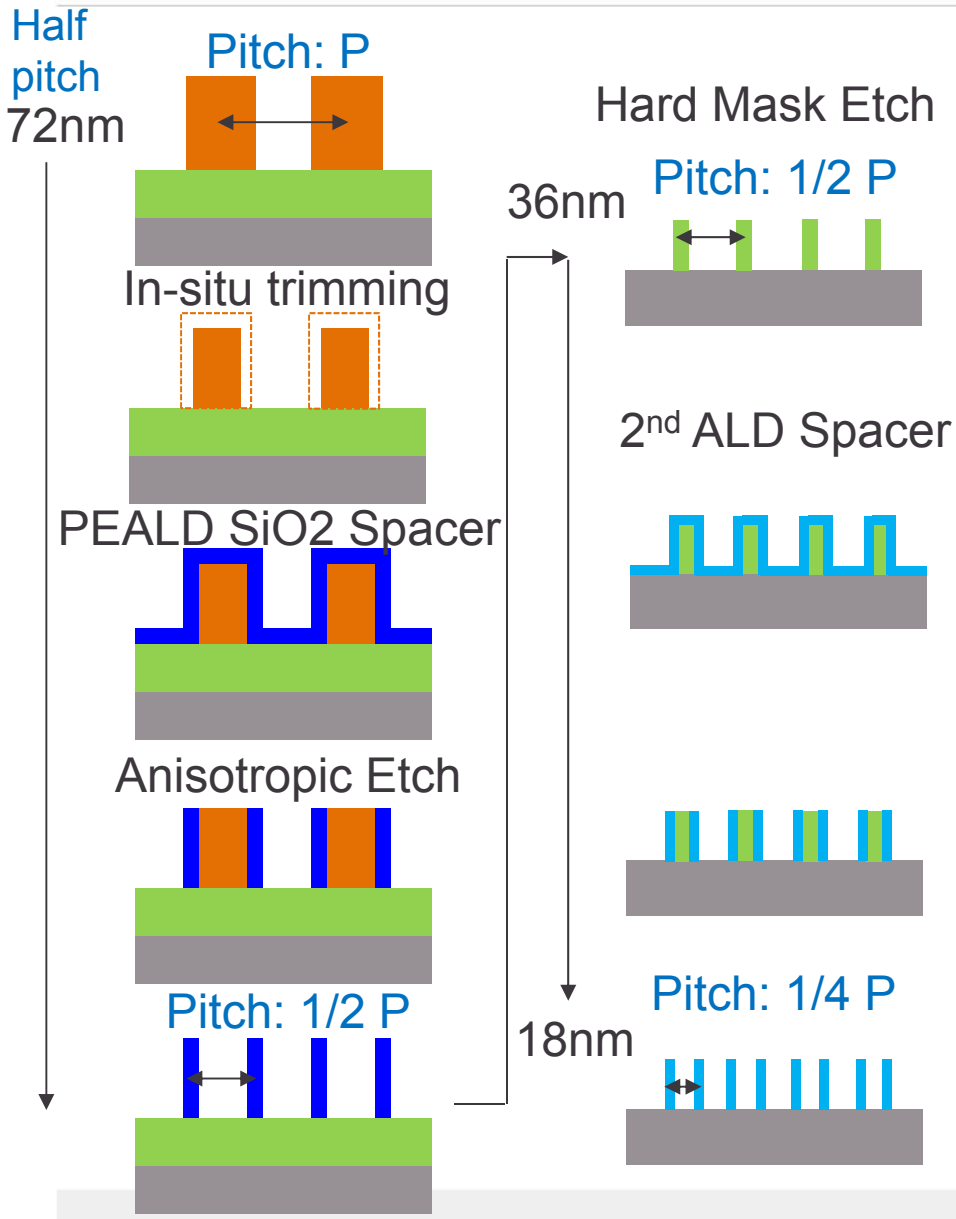
(1-2) High quality PEALD SiO for slit fill

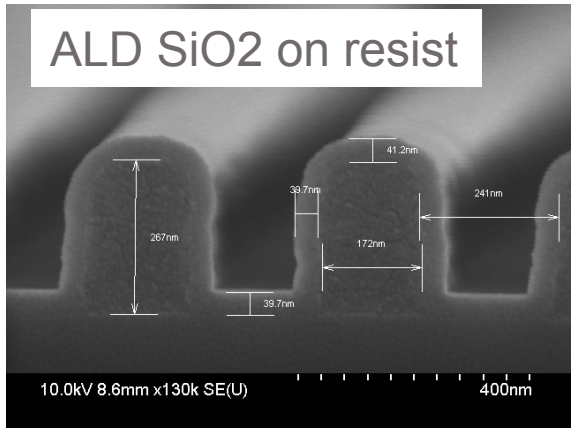


- **High quality conformal SiO**
- **Low temperature process is needed for top select gate separation after WL fill**

TechInsights

ALD FOR SPACER DEFINED DOUBLE/QUADRUPLE PATTERNING



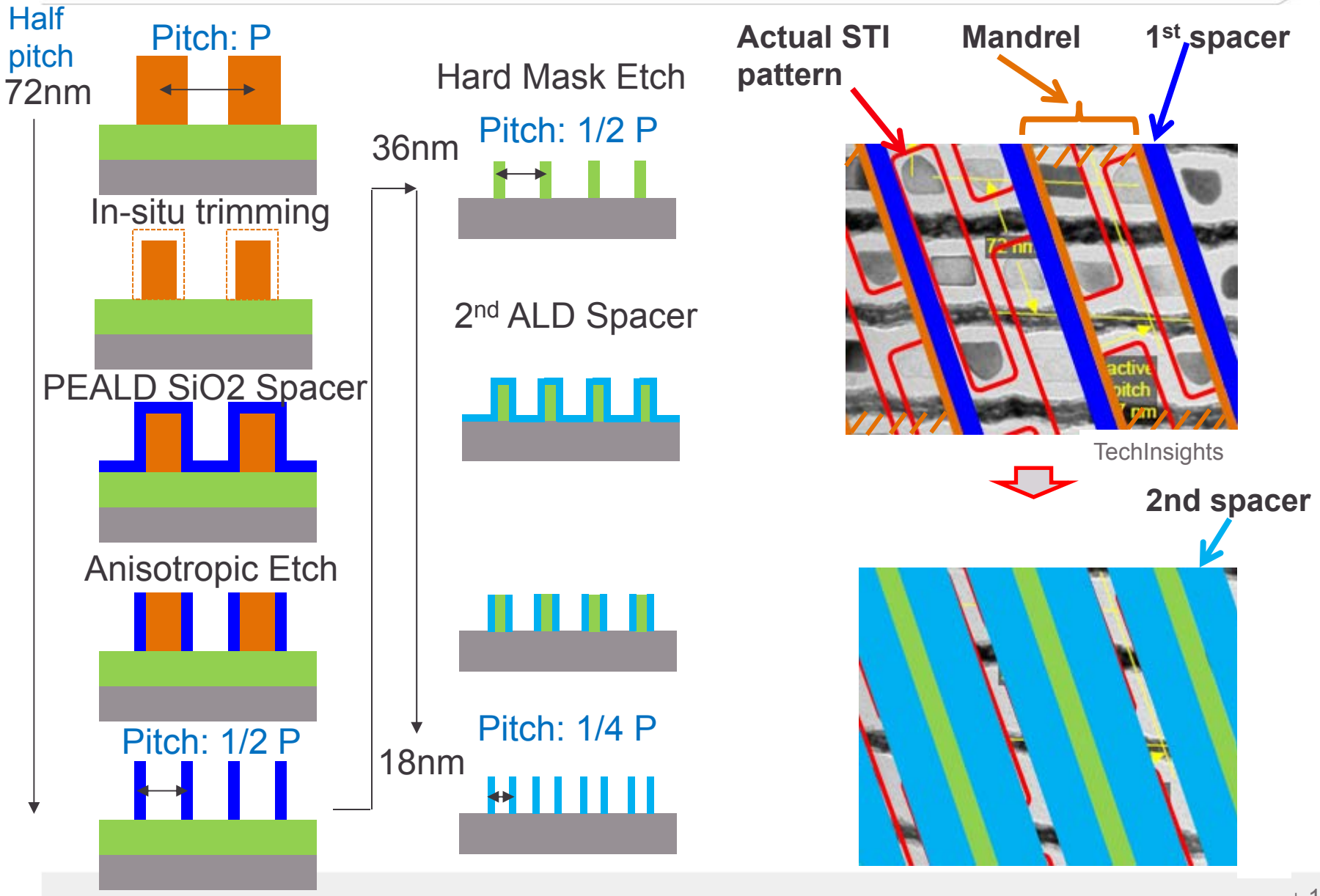


- ✓ **Spacer Defined Double Patterning (SDDP) with ALD in production since 3xnm DRAM and 2xnm Flash**
- ✓ **Spacer Defined Quadruple Pattering (SDQP) in production for 1xnm DRAM**
- ✓ **SDDP/SDQP qualified with 10nm/7nm Logic customers**

Key enablers brought by ALD

- Uniformity: CD control
- Low temperatures (<100C)
- Good step coverage
- Dense film
- In-situ trimming capability
- Extendible to other materials with etch selectivity

ALD FOR SPACER DEFINED QUADRUPLE PATTERNING IN DRAM



PLASMA TRIMMING AND SMOOTHING CAPABILITY

Trimming

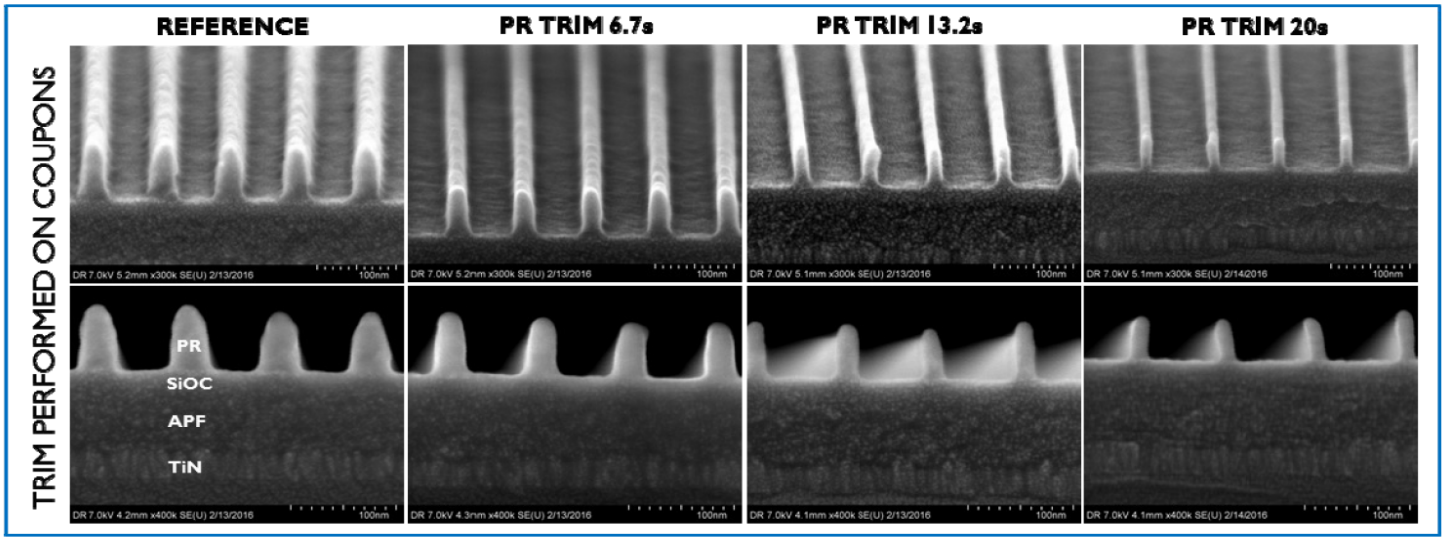
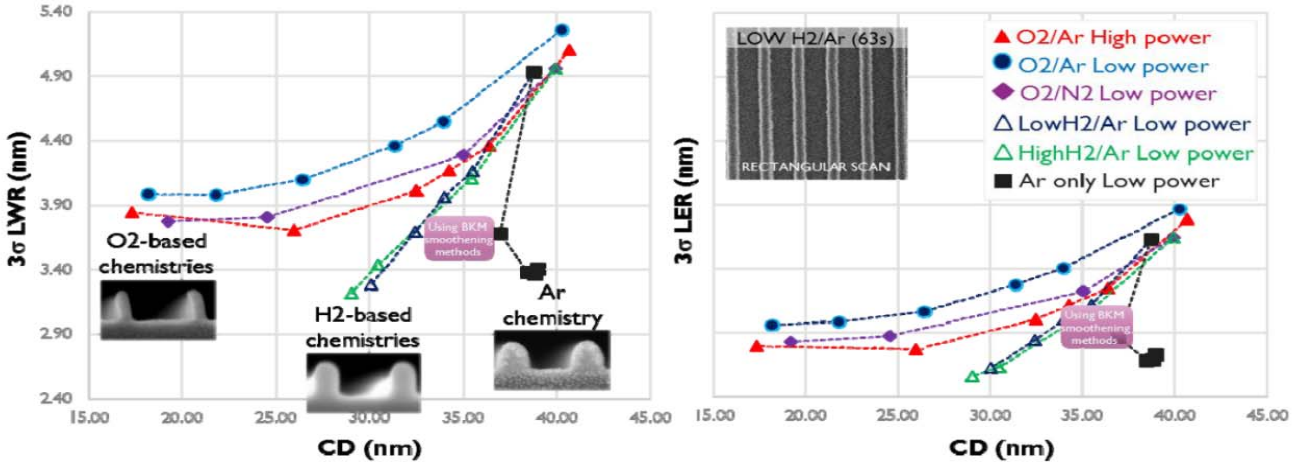


Figure 6. Photoresist line trimming and profile reshaping using O2/Ar low power chemistry

- **Uniformity of PEALD system used to trim and smoothen photoresist**
- **Reshaping of photoresist upon exposure to Ar/O2 plasma**

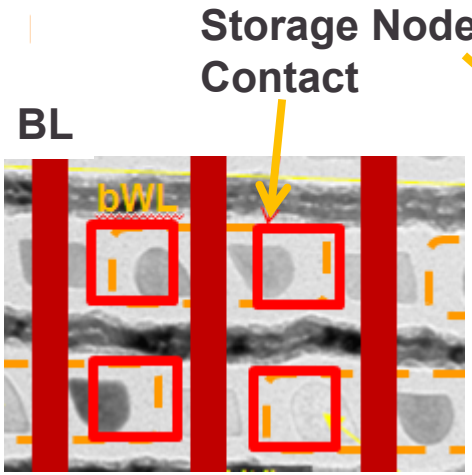
Smoothing



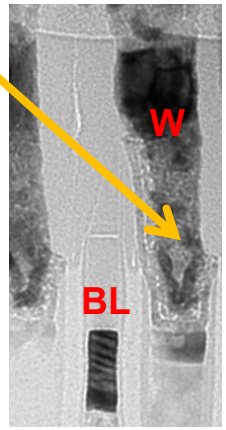
imec 2017 SPIE

ALD FOR SUB-20NM DRAM

1. Bi-directional SDDP for hole patterning, introduced in D1x (LT-PEALD SiO)



Top view (TechInsights)

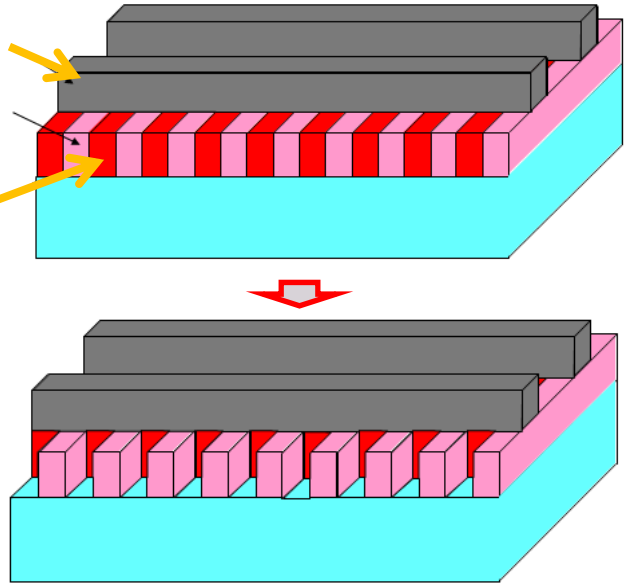


Cross sectional view (TechInsights)

- 2nd SDDP
- PMD SiO after 1st SDDP

Filling

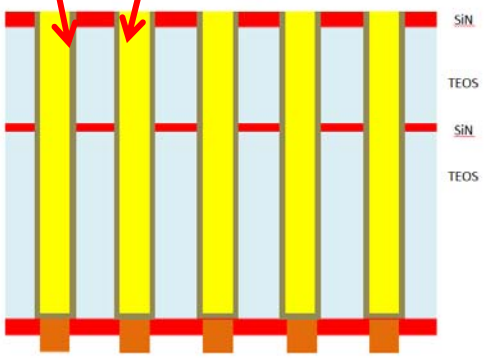
2 times SDDP



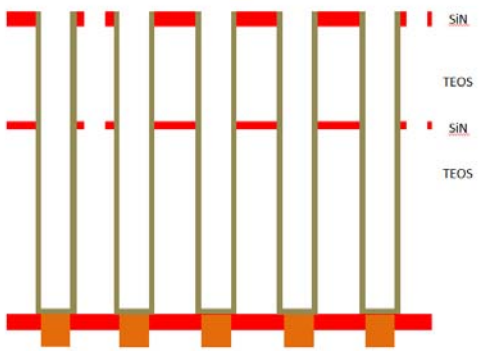
2. Sacrificial SiO (LT-PEALD SiO)

TiN bottom electrode

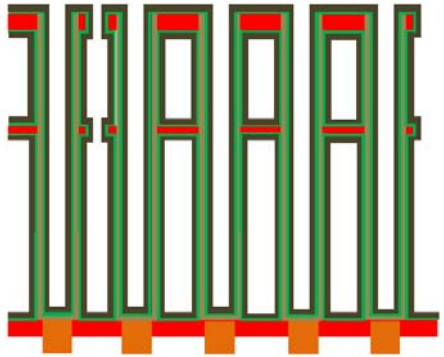
SiO sacrificial fill



Slit formation → SiO removal



Dielectric / metal deposition



ALD METAL HARD MASK WITH TUNABLE ETCH SELECTIVITY

MOx has Dry etching resistance and it is wet strippable.

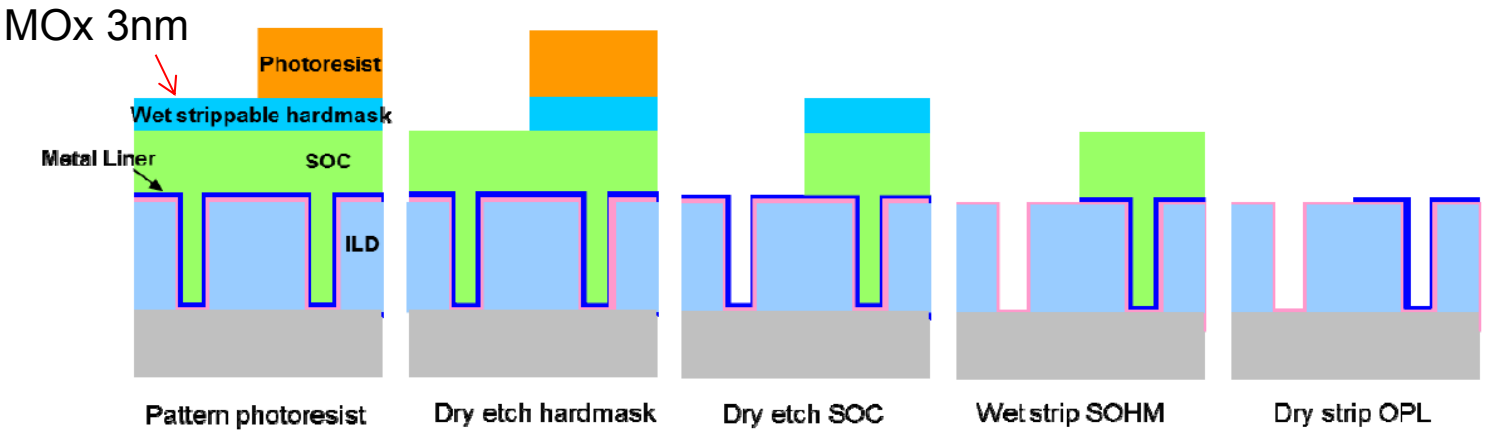
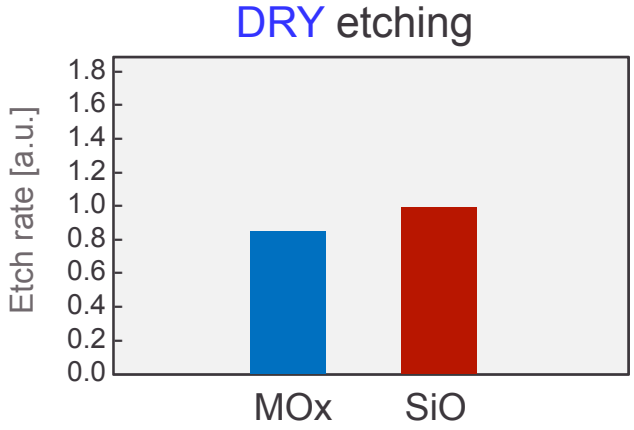
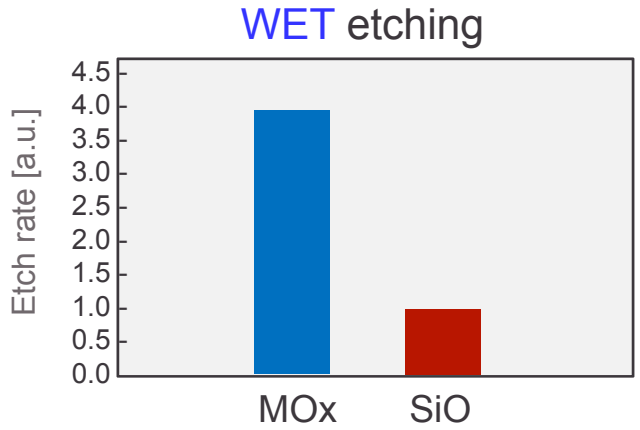


Figure 1: Patterning scheme using a wet-strippable hardmask where it serves as a mask during SOC etch and then wet removal without impact to open area

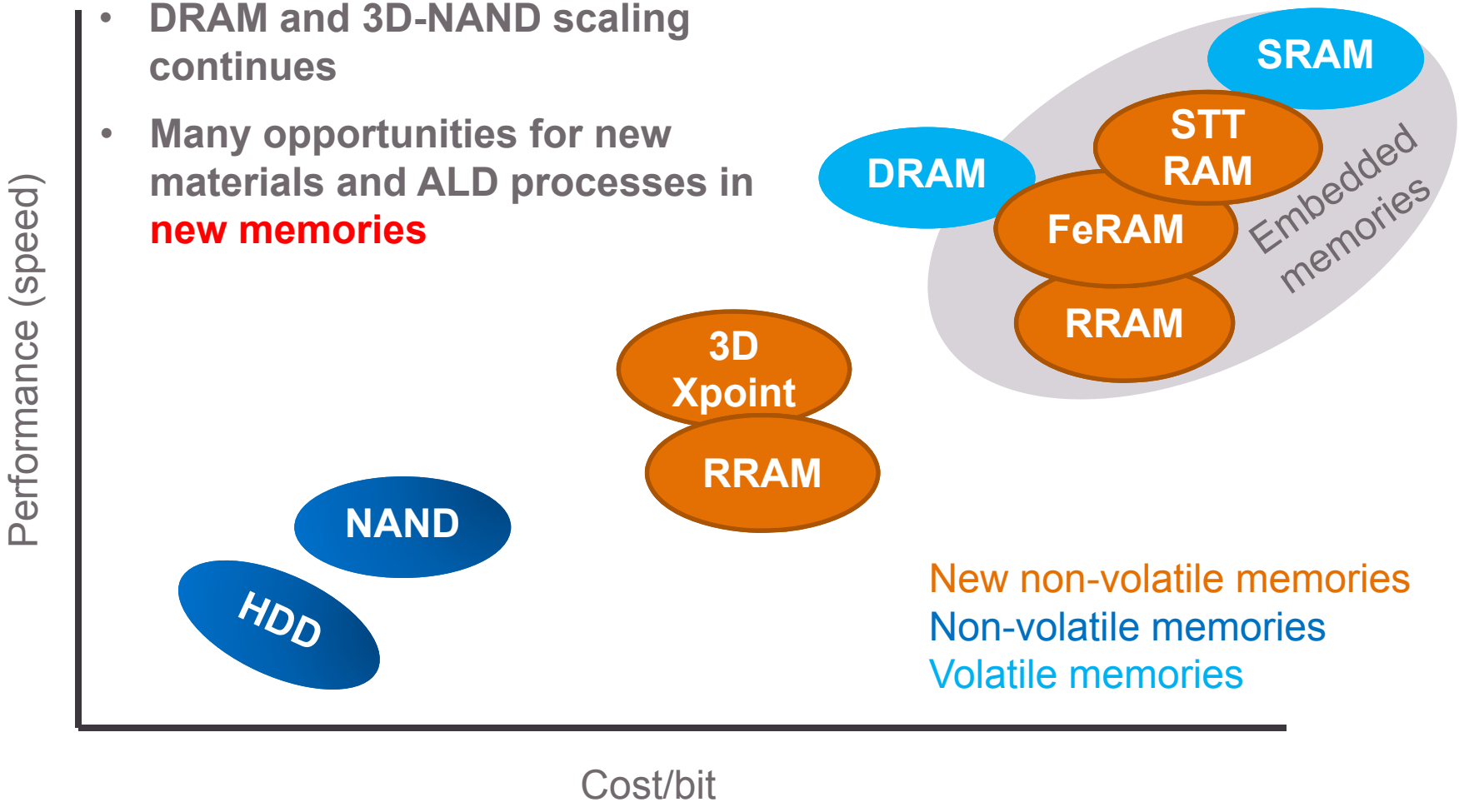




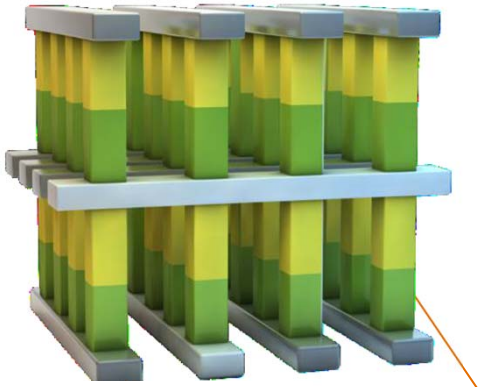
IBM 2017 SPIE

MEMORY HIERARCHY AND FUTURE TRENDS

- **DRAM and 3D-NAND scaling continues**
- **Many opportunities for new materials and ALD processes in new memories**



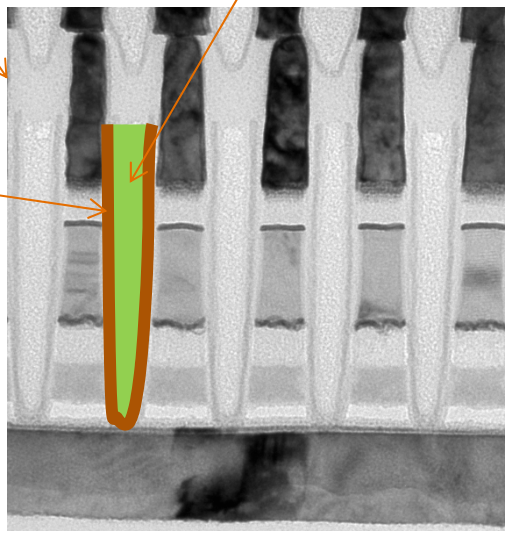
ALD PROCESSES FOR 3D X-POINT



Source:Micron

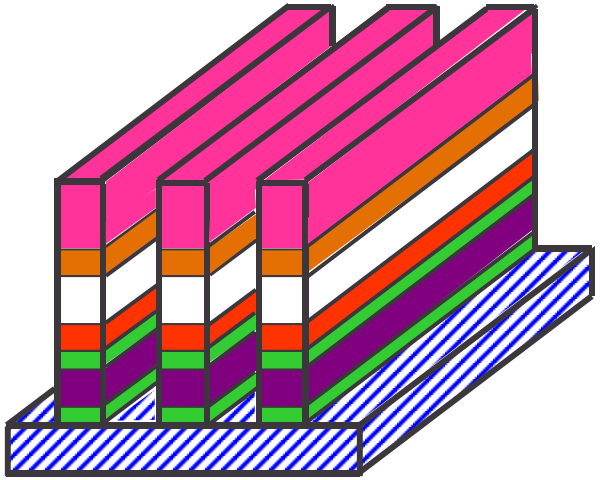
High Quality
Low Temperature
PEALD SiO2
gapfill

High Quality
Low Temperature
PEALD SiO2
liner

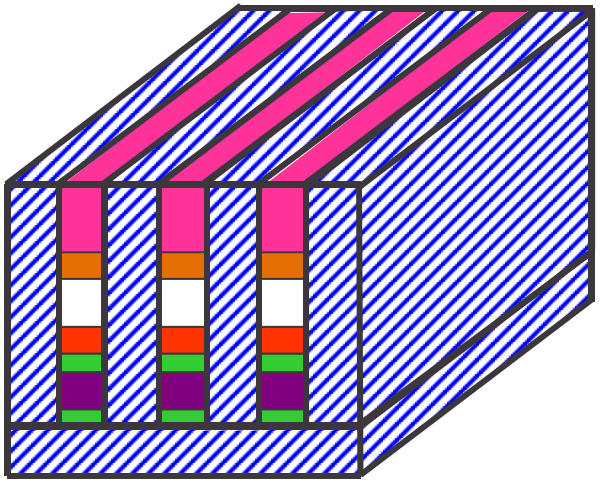


Source: TechInsights

SDDP for WL and BL



PEALD SiO2 liner and gapfill



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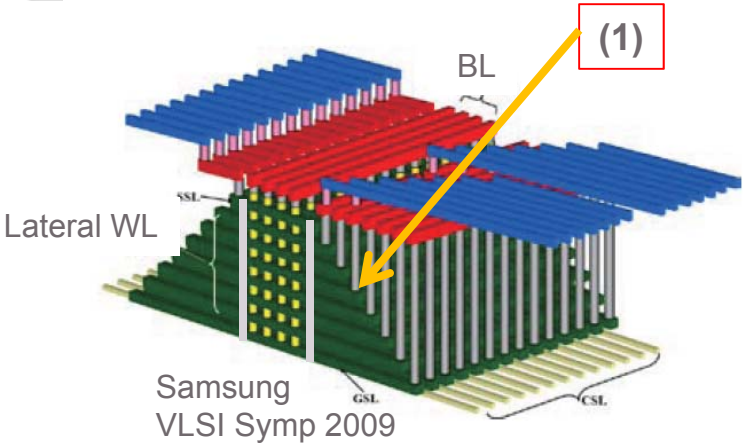
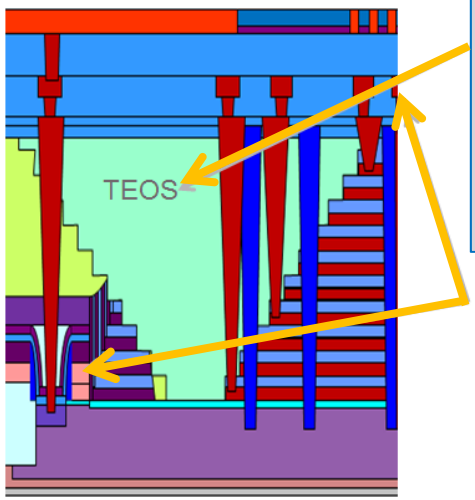
  - Intrepid ES features & benefits

PECVD FOR 3D-NAND APPLICATIONS



(1) PECVD TEOS applications



TEOS
- **High throughput**
- **Good wiw uniformity**
- **High quality**
- **Stress control**

› New applications
- Anti Reflective Layer: SiON
- Amorphous Si
- Amorphous Carbon Hard Mask

OUTLINE

- **New Materials and 3D: Moore's law enablers**
  - ASM technology focus: enabling new materials and new device integration roadmaps
  - Logic scaling
- **ALD**
  - Key strengths of the technology
  - Selected applications in 3D-NAND, DRAM, logic and Emerging Memory
- **PECVD**
- **Vertical Furnace**
- **Epitaxy – Introducing Intrepid® ES™**
  - Epi technology trends
  - Intrepid ES features & benefits

ASM PRODUCTS
FURNACE CVD /DIFFUSION /BATCH ALD

A412 PLUS

- Dual boat/dual reactor system
- Clustering of different applications between reactors possible – only vertical furnace in the market with this capability
- Up to 150 product wafer load size

A400 for More than Moore Devices

- Dual boat/dual reactor system
- Simultaneous handling of Dual size wafers

Applications:

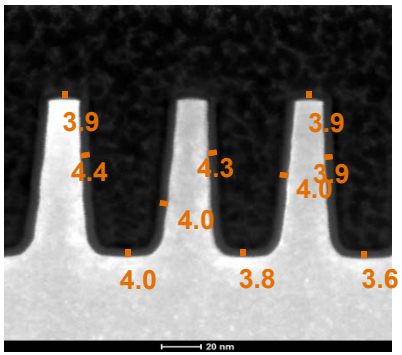
- Full range of applications for Logic, Memory, Power and MEMS Devices

- LPCVD Silicon, SiN, TEOS, HTO
- Diffusion, Anneal, Cure, Reactive Cure
- Batch ALD (AlO, AlN, TiN, SiN, SiO, etc)

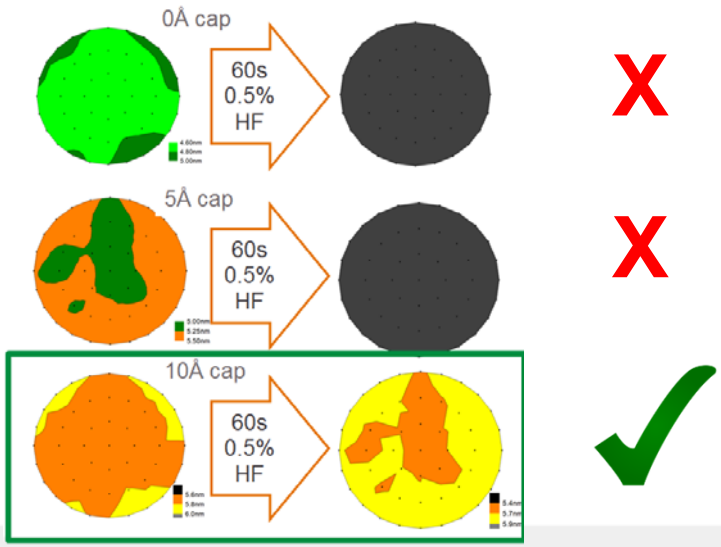
A400/A412 FURNACE - INNOVATION

Example 1: Novel Etch Stop Layer (ESL)

› Scaling of **Logic** devices requires conformal Nanolayers with high etch resistivity



› We developed a novel 1 nm thin ESL:



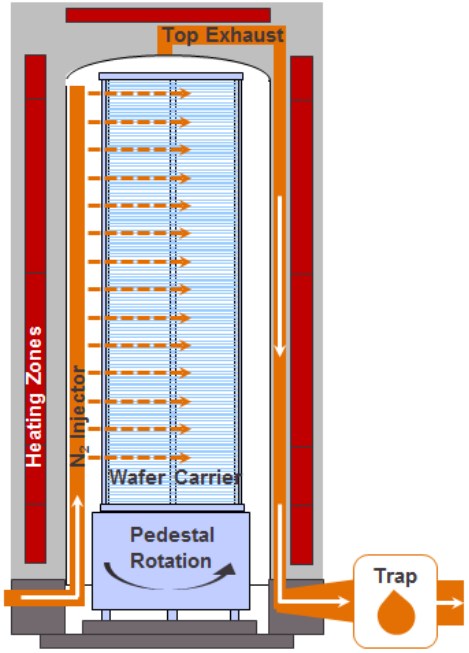
X

X

✓

Example 2: Polylmid Cure

› Polylmid films are key components in **Wafer Level Packaging**. A highly uniform low temperature anneal process that cures the polylmid films requires control of low O_2 and moisture as well as dedicated wafer handling for “Molded Wafers” with Known Good Dies (KGD).



A412 Polyimide Cure
reactor cross section

OUTLINE

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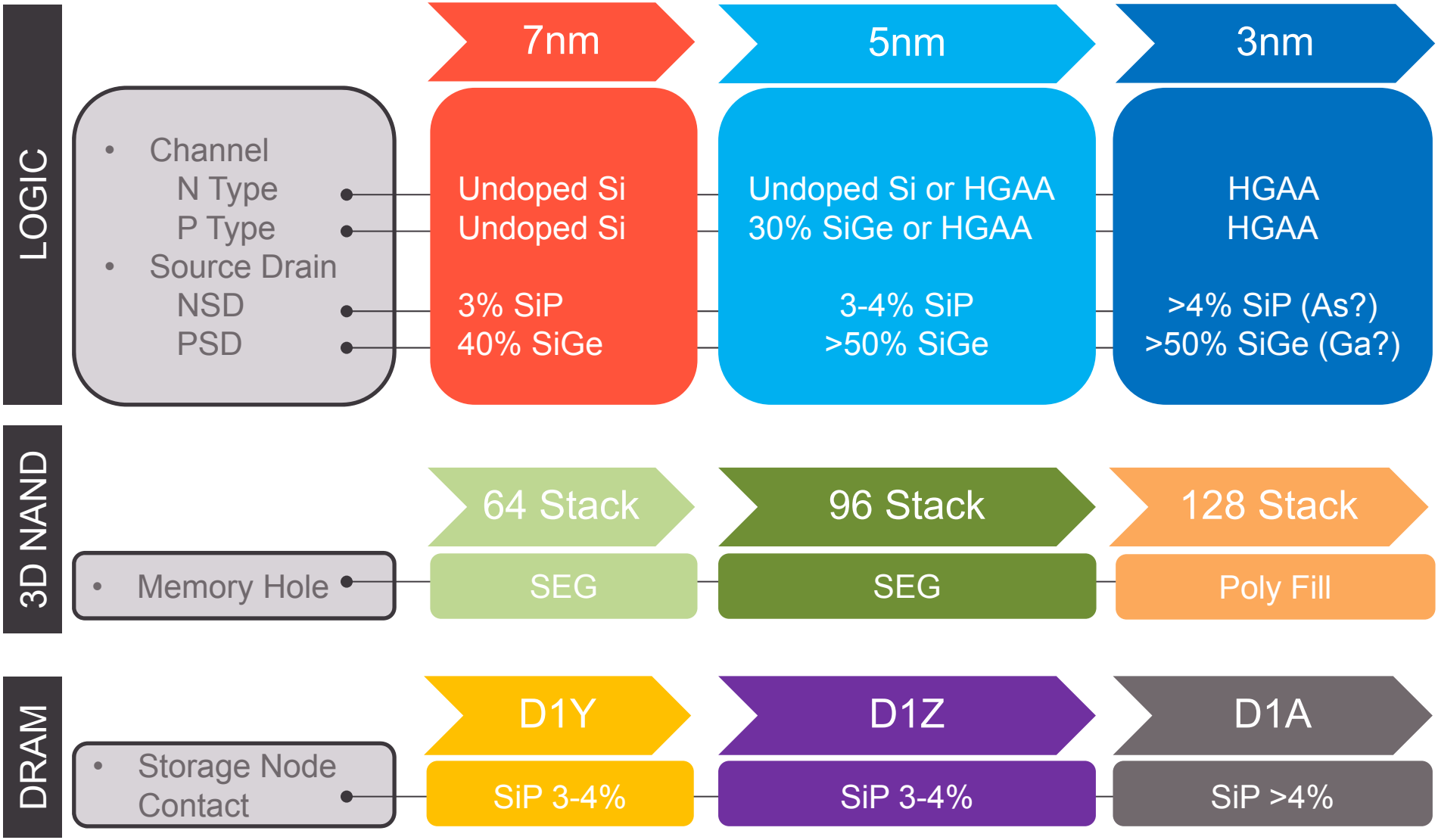
  - Epi technology trends
  - Intrepid ES features & benefits

EPI PROCESS ROADMAP



INTREPID ES: APPLICATION LIBRARY

LOGIC

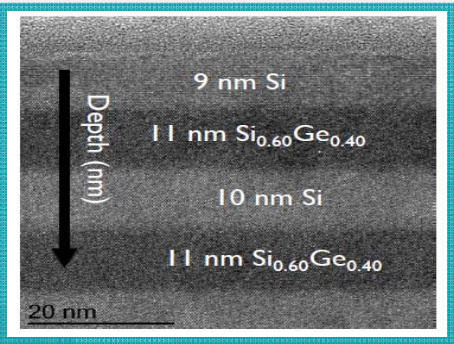
Channel
- N-type
- P-type
- Si / SiGe HGAA

Source Drain
- NSD
- PSD

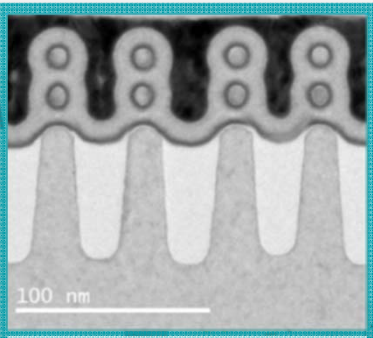
MEMORY

3D NAND
- Channel hole

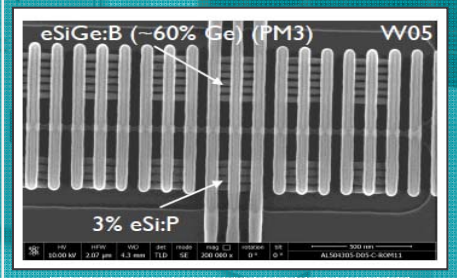
DRAM
- Storage node contact



SiGe / Si gate all around device
Source: imec



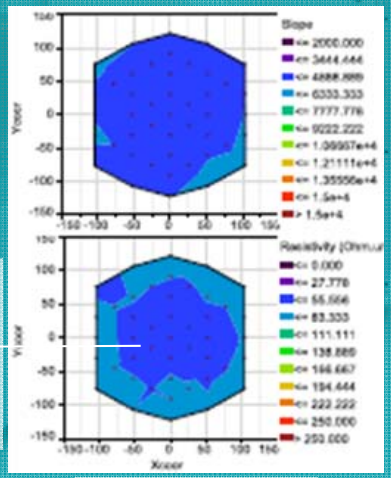
Si nanowire: 8nm radius
Source: imec



Excellent uniformity, SiP (3% P)
Source: imec

4-Fin resistance (Ω/µm)

Contact resistivity (Ω cm)



ASM-imec SiP

A library of applications are available on the Intrepid ES

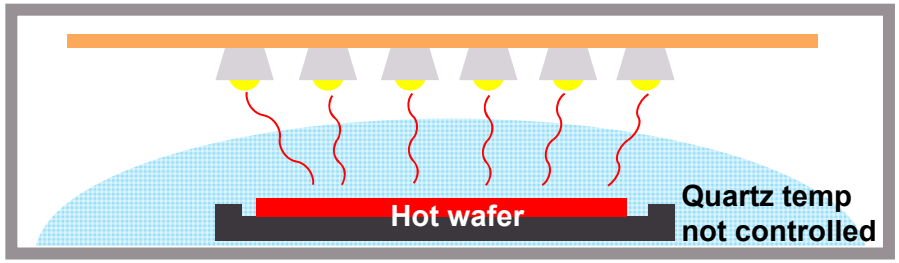
INTREPID ES: KEY FEATURES

- **Low Chamber Volume**
- **Dual Temperature Measurement: Pyrometer / TC**
- **Isothermal Quartz Chamber: Closed Loop Control**

Intrepid ES delivers *isothermal* process modules for improved within wafer and wafer-to-wafer performance with the highest throughput

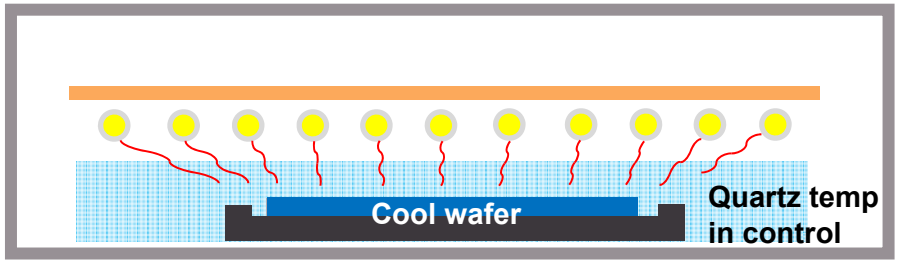
ADVANCEMENTS IN EPITAXY: LOW TEMPERATURE

Conventional Epi



- Hot temperature processes: > 900°C
- Pyrometer control for temperature is possible
- Wafer temperature dominates – process environment not critical

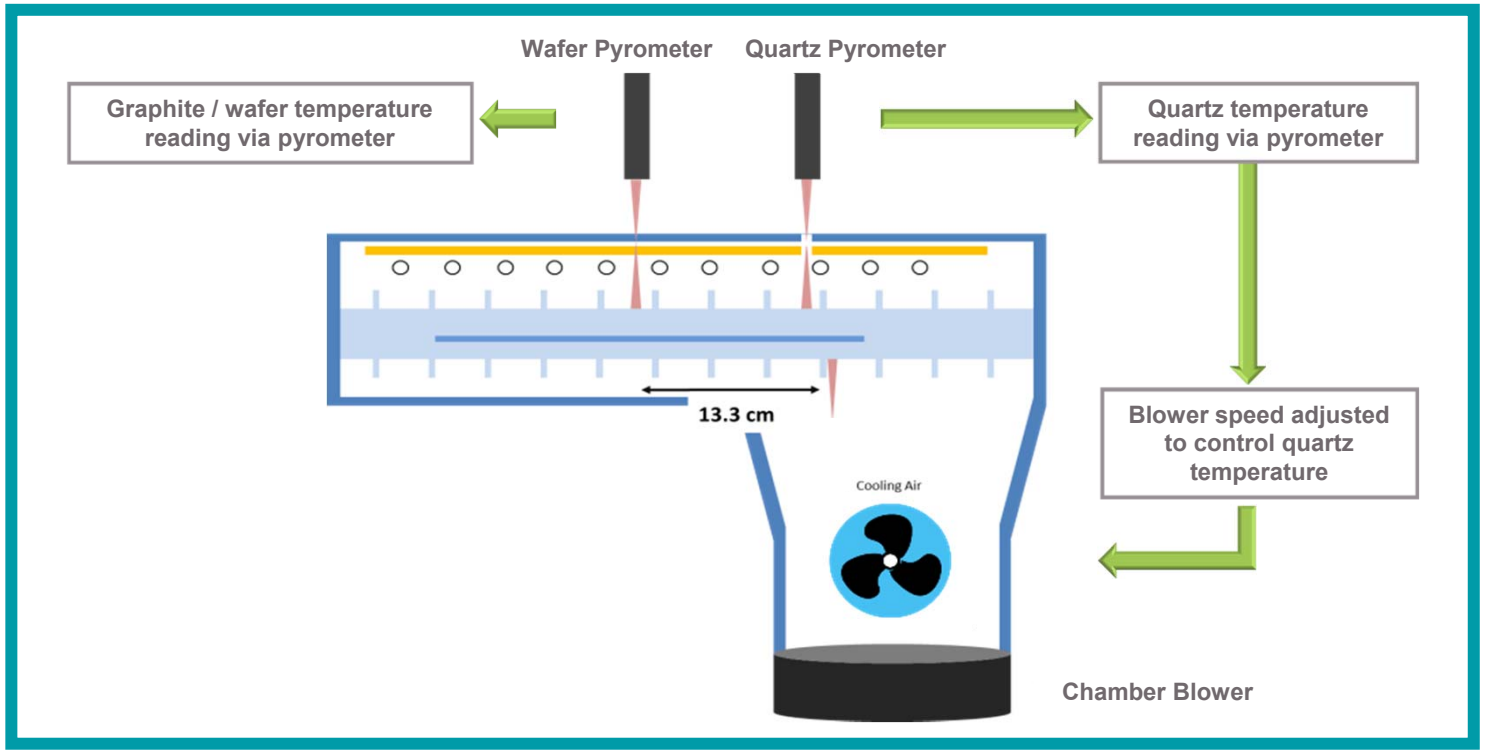
Advanced Epi



- Low temperature processes: 400°C – 700°C
- Pyrometers are not accurate in this temperature range – TCs needed < 550°C
- Quartz temperature and chamber environment control is critical

Low temperature Epi processing driving stringent reactor performance and control requirements

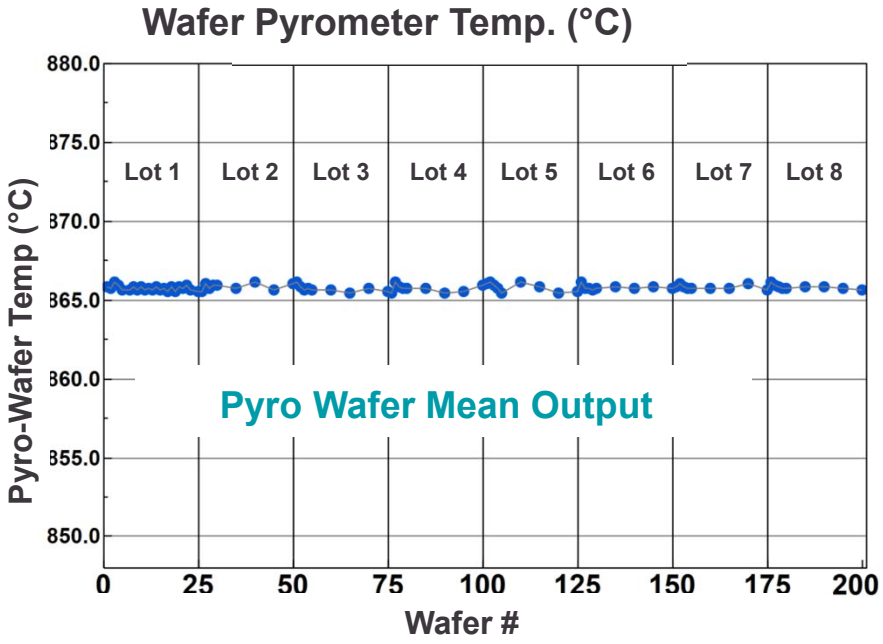
INTREPID ES KEY FEATURES: TEMPERATURE CONTROL

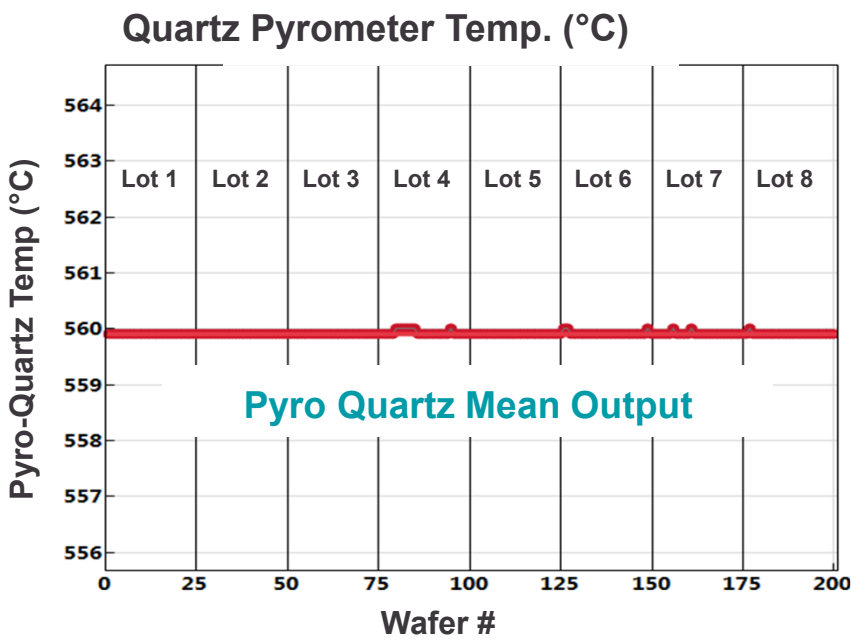


Temperature Control	ASM's "Inside Out" Approach
Wafer Temperature Control	Direct Control
Quartz Temperature Control	Direct Control

ASM chamber design utilizes both TC- and pyrometer-based temp. measurement

PYRO TEMPERATURE (°C): 200X WAFER CLEAN





	Pyro-Wafer Temp. (°C)
Mean	865.7
St. Dev.	0.18
Min.	865.4
Max.	866.1
Range	± 0.4

	Pyro-Quartz Temp. (°C)
Mean	559.9
St. Dev.	0.02
Min.	559.9
Max.	560.0
Range	± 0.1

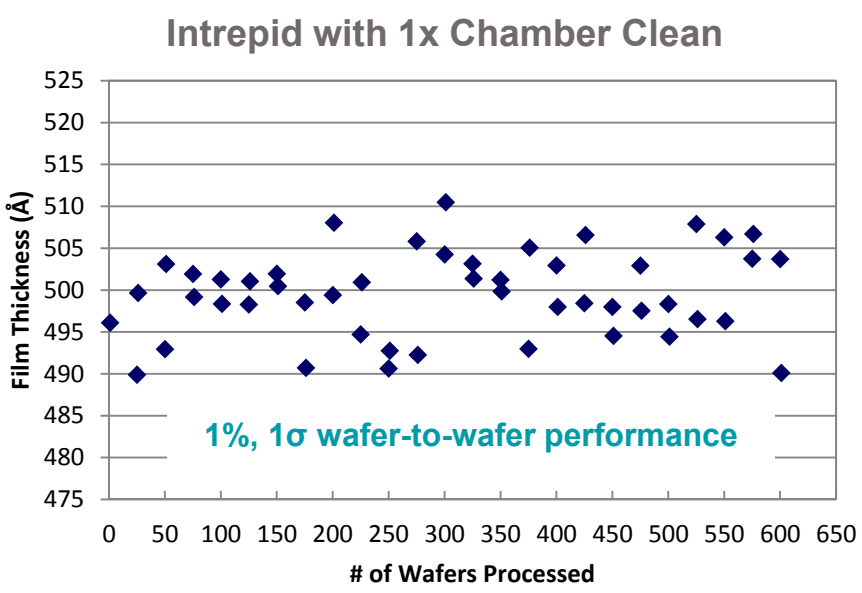
<0.8 degree wafer temp. repeatability over entire 200 wafer run

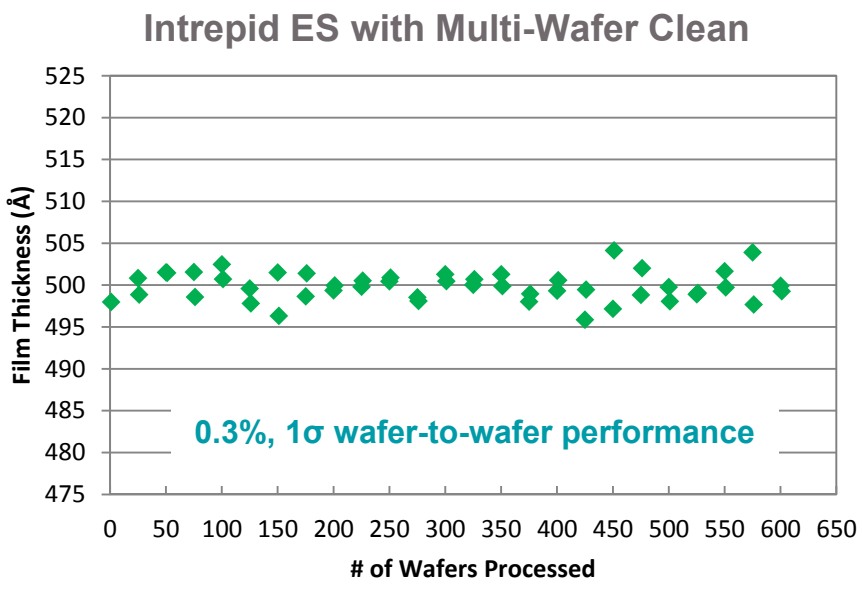
TRENDS IN EPITAXY: ASM SOLUTIONS

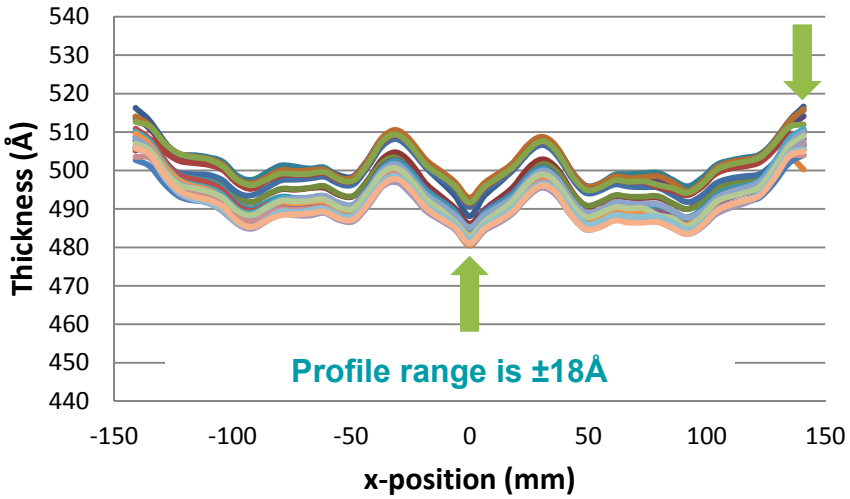
Epi Trends	ASM Solutions
Logic: GAA → stack layers with precise interface control (Si / SiGe)	Small chamber volume
Low temp. processing	TC control (pyrometry limitations <550°C) + isothermal kit Higher GR achievable due to better precursor utilization and lower dilution
Memory: 3D NAND → low cost / high throughput	Isothermal kit with multi-wafer clean
Pre-clean evolution	SiO_2 + $SiGeO_x$ and interfacial carbon removal (Epi platform integrated with Previum pre-clean)

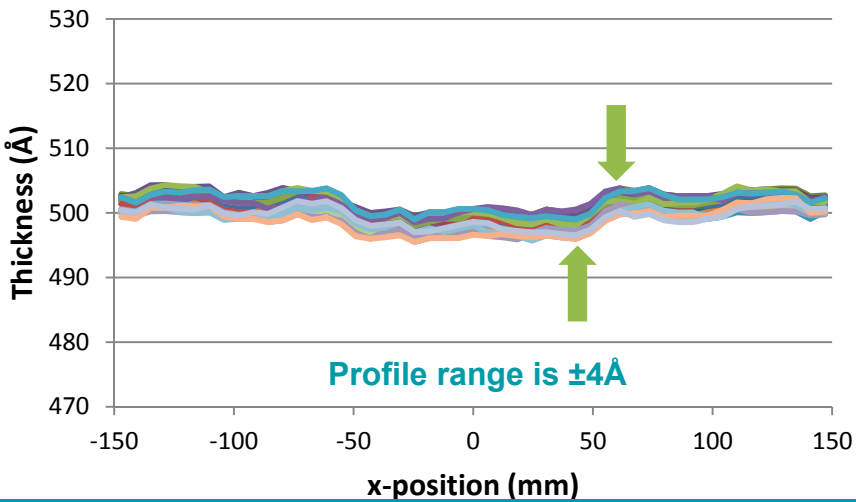
ASM continues to develop innovations to address Epi technology trends

INTREPID ES: ENHANCED STABILITY



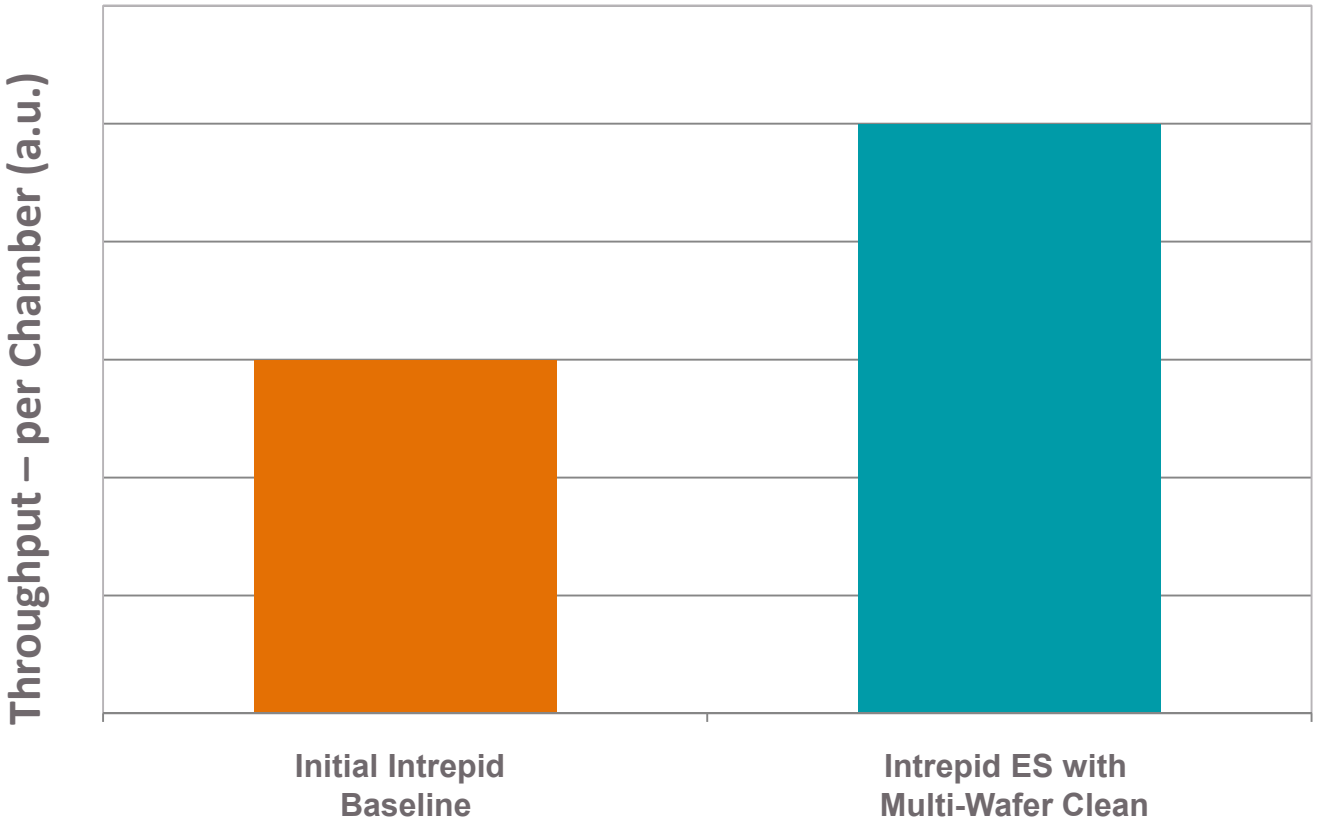






Enhanced stability delivered with the implementation of the isothermal kit

INTREPID ES HVM SOLUTION: THROUGHPUT

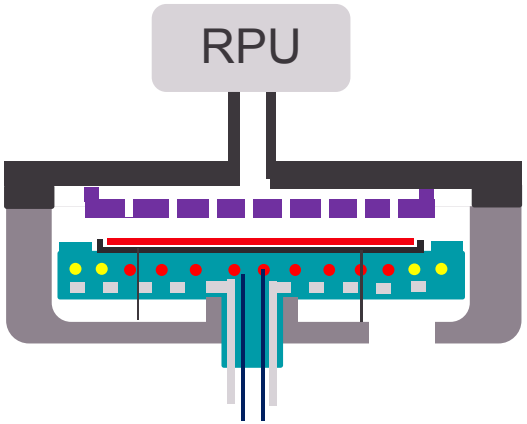


BACK

Isothermal kit and multi-wafer clean deliver higher throughput for HVM

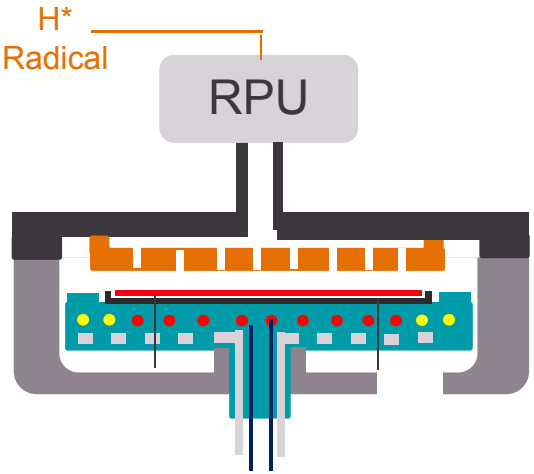
PREVIUM: INTEGRATED SURFACE PRE-CLEAN

Previum

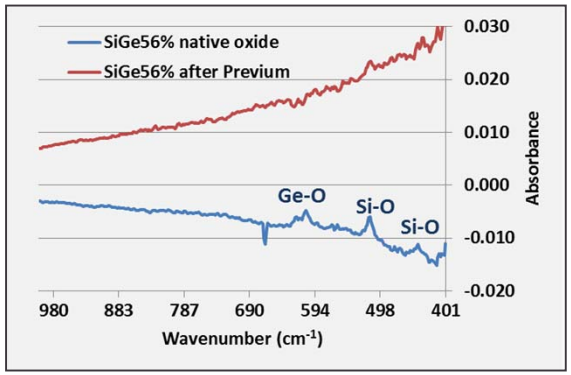


- ✓ In-situ conversion / sublimation for SiO_2

Previum for C Removal



$Si_{0.44}Ge_{0.56}$ oxide removal in Previum (FTIR analysis)



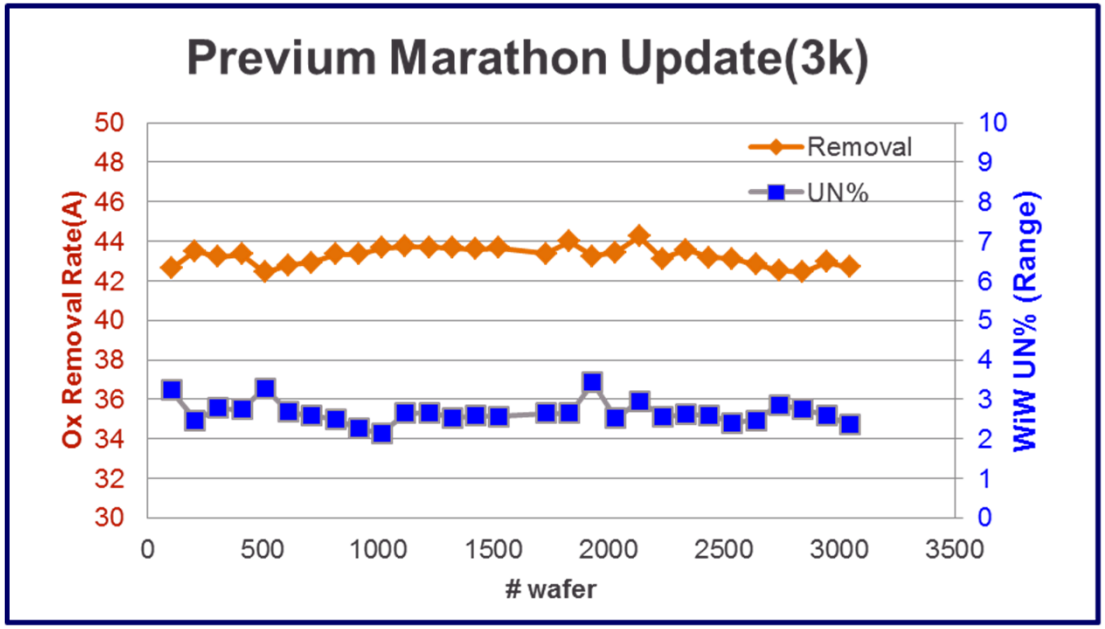
Optimized pre-clean process to remove $SiGeO_x$

- ✓ In-situ conversion / sublimation for SiO_2 AND $SiGeO_x$
- ✓ H* radical for carbon removal
- ✓ Leverage ASM strength in high temp. chamber technology

Previum pre-clean chambers used with Intrepid ES Epi chambers for advanced logic and memory development

PREVIUM PERFORMANCE

Oxide Removal



Oxide Removal (Å)	43.3
WtW Removal Unif. (%)	1.1%

Particle Performance

Monitor Wafer No.	Adders
258	0
512	0
765	2
1018	0
1272	1
1526	2
1779	3
2033	0
2286	4
2539	4
2792	8
3046	1

Average adders: 2.1, >45nm

Stable oxide removal demonstrated with low defectivity

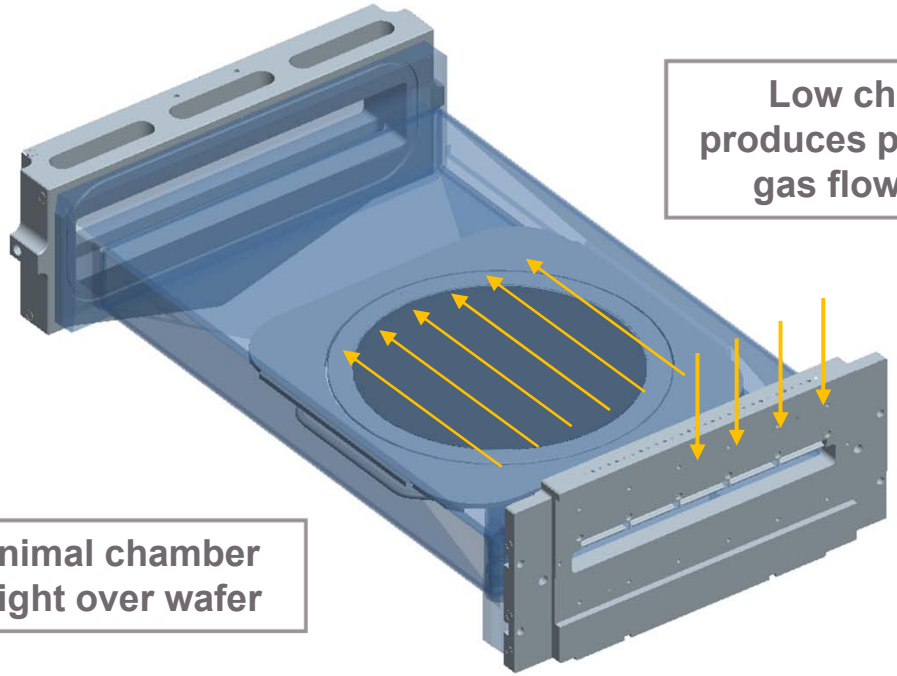
INTREPID ES

- Delivers improved within-wafer and wafer-to-wafer performance with the highest throughputs
- Qualified for production at a leading-edge foundry customer, targeting production applications in other industry segments
- Integrated Previum pre-clean to address current and future surface pre-treatment requirements

DRIVE INNOVATION • DELIVER EXCELLENCE

INTREPID ES KEY FEATURES: CHAMBER DESIGN

Chamber Design



Low chamber volume produces predictable laminar gas flow over the wafer

Minimal chamber height over wafer

Small Volume = Small Precursor Flows

- Low Gas Consumption
- Short Chamber Cleans
- Small Footprint Abatement

BACK

Reactor design enables *high productivity* and *low cost of ownership*

DRIVE INNOVATION • DELIVER EXCELLENCE