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Fundamental Theory of PMOS Low-Dropout Voltage Regulators

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Fundamental Theory of PMOS Low-Dropout Voltage Regulators

By Tom Kugelstadt

ABSTRACT

This report presents a fundamental understanding on the theory of low-dropout voltage regulators using a PMOS FET as the pass element to adjust the output current to the load requirements.

Fundamentals

A voltage regulator is a constant voltage source that adjusts its internal resistance to any occurring changes of load resistance to provide a constant voltage at the regulator output.

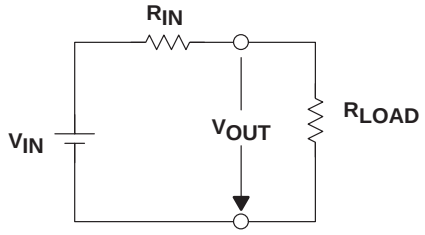

Figure 1. Constant-Voltage Source

The internal resistance of a constant voltage source (Figure 1) must be significantly smaller than the external load resistor ($R_{IN} << R_{LOAD}$) to ensure a constant output voltage over a certain range of load changes.

The output voltage of a voltage source is calculated as:

$$V_{OUT} = V_{IN} \times \frac{1}{1 + \frac{R_{IN}}{R_{LOAD}}} \quad (1)$$

Under no-load condition ($R_{LOAD}= \infty$), the maximum output voltage possible is equal to the input voltage ($V_{OUT\text{-}MAX} = V_{IN}$). As the load increases, the output voltage drops from its imum value and introduces an output-voltage error E_{VO}. This error E_{VO} is defined as the percentage difference between V_{OUT} under no-load condition ($V_{OUT\text{-}MAX}$), and V_{OUT} under load condition ($V_{OUT\text{-}LOAD}$).

$$E_{VO} = \frac{V_{OUT\text{-}MAX} - V_{OUT\text{-}LOAD}}{V_{OUT\text{-}MAX}} \times 100\% \quad (2)$$

When replacing $V_{OUT\text{-}MAX}$ with V_{IN} and substituting $V_{OUT\text{-}LOAD}$ with the value in equation 1, the voltage error is expressed through the resistor ratio of R_{IN} to R_{LOAD}:

$$E_{VO} = \frac{R_{IN}}{R_{IN} + R_{LOAD}} \times 100\% \quad (3)$$

A plot of the voltage error over a series of R_{LOAD}-to-R_{IN} ratios confirms that the output voltage error E_{VO} increases with decreasing load resistance R_{LOAD}, as shown in Figure 2.

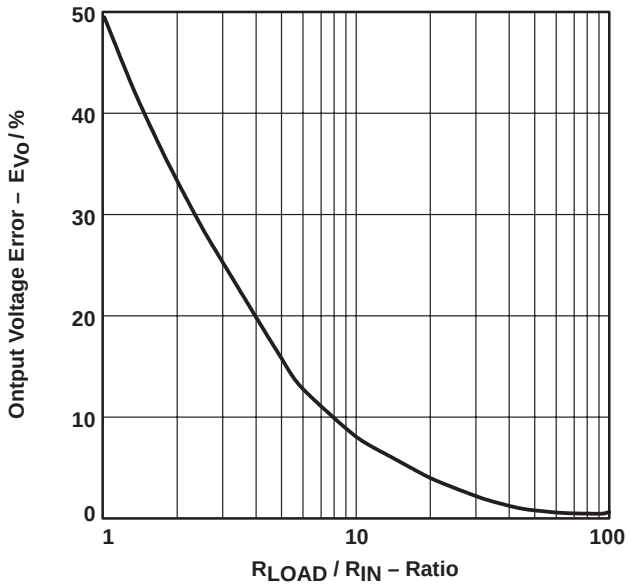

Figure 2. Output-Voltage Error vs Load Resistance

To minimize the error we need a circuit that senses any occurring load changes and, via some kind of feedback, adjusts a variable internal resistor to keep a constant ratio of internal-resistance to load-resistance: $R_{IN}/R_{LOAD} = k$.

$$R_{IN} = R_{LOAD} \times k \tag{4}$$

When this is true, R_{IN} would follow R_{LOAD} in a linear relation: $R_{IN} = kR_{LOAD}$. This circuit is shown in Figure 3.

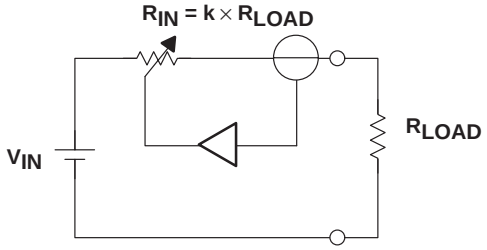

Figure 3. Linear Relation Between R_{IN} and R_{LOAD}

A circuit that accomplishes this is basically a linear-voltage regulator, and is illustrated in Figure 4.

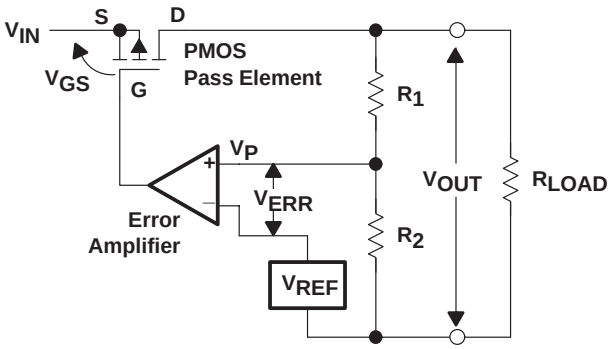

Figure 4. Basic Linear-Voltage Regulator

In the linear-voltage regulator illustrated in Figure 4, we can identify the following building blocks:

- **The voltage reference**, which is the starting point of all regulators. This is usually of the bandgap-type, since this kind of reference has the ability to work down to low supply voltages, and provides enough accuracy and thermal stability to meet the less-stringent performance requirements of regulators. Bandgaps typically have an initial error of 0.5% – 1.0% and a temperature coefficient of 25 – 50 ppm/°C.
- **The error amplifier**, whose function is to take a scaled-down version of the output, $V_P = V_{OUT} R_1/(R_1 + R_2)$, compare it against the reference voltage ($V_P = V_{REF}$), and adjust $V_{OUT,}$ via the series-pass element, to the value required to drive the error signal ($V_{ERR} = V_P - V_{REF}$) as close as possible to zero. Setting $V_{REF} = V_P$ yields :

  $$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times V_{REF} \quad (5)$$

  This holds true only if V_{IN} is sufficiently high to keep the error amplifier and the pass element from saturating.
- **The feedback network**, whose function is to scale V_{OUT} to a value suitable for comparison against V_{REF} by the error amplifier. Since V_{REF} is fixed, the only way to program the value of V_{OUT} is by adjusting the ratio R_2 / R_1.
- **The series-pass element**, whose function is to boost the output-current capabilities of the error amplifier to the higher levels required by the load. This involves transferring large currents from the source V_{IN} to the load under the low–power supervision of the error amplifier. A suitable pass element to carry out this task is a PMOS enhancement FET. A PMOS FET has the two p-islands for the source and the drain terminals embedded in an n-substrate, as shown in Figure 5a. The substrate is connected to the source, which usually has the most positive potential. The drain receives the most negative potential. As the PMOS name indicates, the device uses p-type conductivity, which is established by applying a voltage to the gate that is negative relative to the source.

  The holes, which are the minority carriers in the n-substrate, are attracted by the negative gate electrode. Moving towards the upper region between the two p-islands, the holes now become free-charge carriers, establishing a p-conductive bridge between source and drain. This way, the conductivity of the bridge, and with it the drain current I_D, are controlled by the gate-source voltage, V_{GS}.

  Since this type of FET enhances its conductivity with increasing V_{GS}, it is called an *enhancement* or *normally-off* type (see Figure 5b).

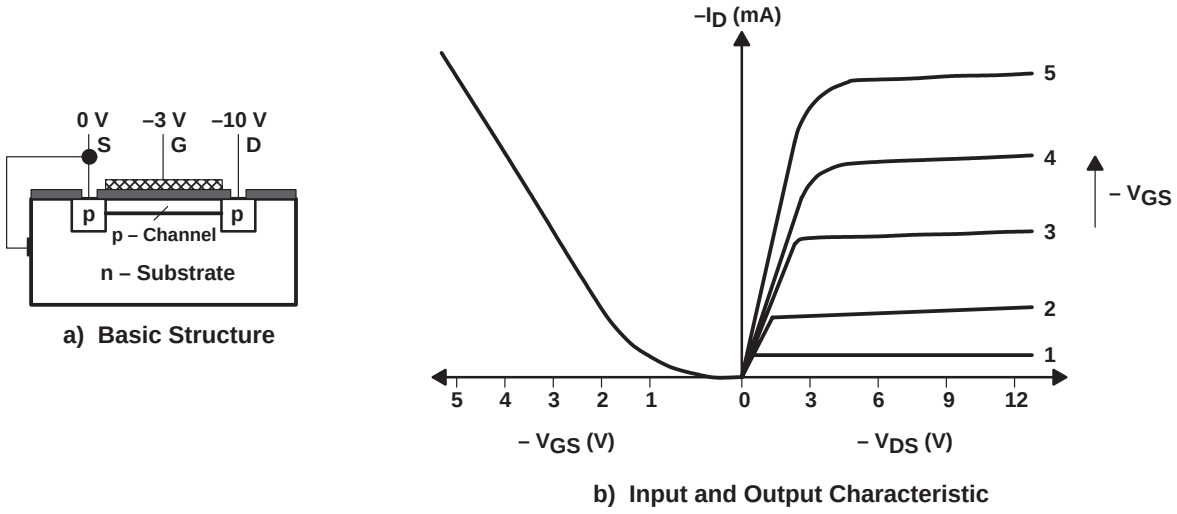

Figure 5. PMOS Enhancement FET

Regulator Sequence

The following is a description of the regulation sequence when R_{LOAD} drops.

When the load resistance drops, the output voltage falls from V_{OUT1} to $V_{OUT2,}$ and the voltage across the pass element rises from $–V_{DS1}$ to $–V_{DS2}$. V_P, which is a scaled down version of $V_{OUT,}$ falls significantly below V_{REF} causing the gate-source voltage to jump from $–V_{GS1}$ to $–V_{GS2}$.

The PMOS FET now conducts harder, increasing the output current from I_{OUT1} to I_{OUT2}. The output voltage and, by virtue of V_P, the error voltage start to recover. The gate voltage increases gradually to $–V_{GS3}$, thus causing the increased output current I_{OUT3} to generate an output voltage $V_{OUT.}$ When this output voltage is scaled down via R_1 and R_2, the result is a zero-error voltage $V_{ERR} = 0$.

The output characteristic illustrated in Figure 8 confirms the regulation sequence. When R_{LOAD} drops, the PMOS FET operating point jumps from P_1 to P_2 and then regulates to P_3.

Regulation Sequence When R_{LOAD} Drops

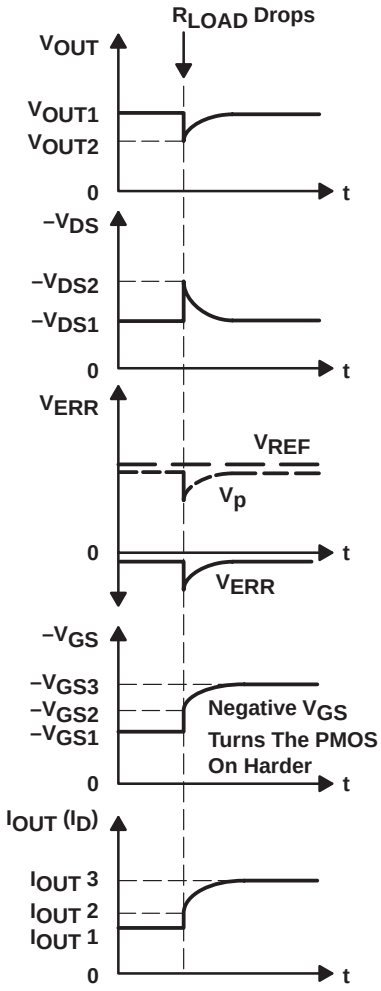

Figure 6. Regulation Sequence When R_{LOAD} Drops

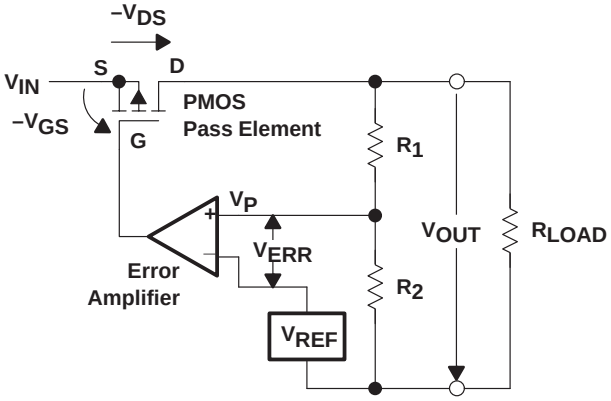

Figure 7. Regulator Block Diagram

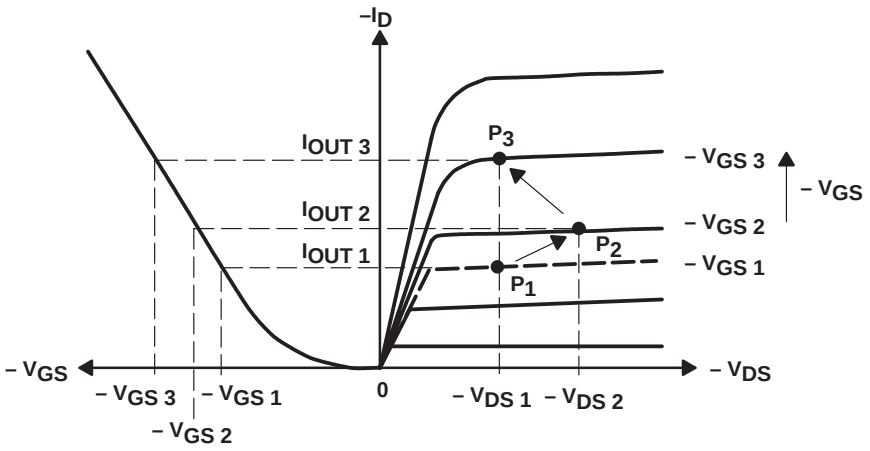

Figure 8. PMOS Input/Output Characteristic

For a given quiescent point P_N where the output voltage has been stabilized (that is, V_{OUT} and V_{DS} are constant), we can define the internal resistance of the PMOS FET, and the load resistance in general terms as follows:

$$R_{IN\,N} = \frac{V_{DS}}{I_{OUT\,N}} \quad \textit{and} \quad R_{LOAD} = \frac{V_{OUT\,N}}{I_{OUT\,N}}$$

Solving both equations for I_{OUT} yields: $I_{OUT\,N} = \dfrac{V_{DS}}{R_{IN\,N}} = \dfrac{V_{OUT}}{R_{LOAD\,N}}$

Solving for R_{IN} results in: $R_{IN\,N} = R_{LOAD\,N} \times \dfrac{V_{DS}}{V_{OUT}}$ (6)

With $k = V_{DS}/V_{OUT}$, Equation 6 provides the linear relation required by a linear voltage regulator.