High Voltage Power MOSFET switching parameters: Testing Methods for Guaranteeing datasheet limits

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Introduction

Power MOSFET datasheets will usually show typical and min-max values for R_g, C_{iss}, C_{rss}, C_{oss}, and also show values for gate charge broken down into Q_{gs}, Q_{gd}, Q_g. It is also customary to show values for switching times during resistive switching, $t_{d(on)}$, t_{rise}, $t_{d(off)}$, t_{fall}. (For a glossary of terms, see appendix I)

It is well known that the device parameters Q_{gs}, Q_{gd}, Q_g have a one-to-one correlation with the parameters C_{iss} and C_{rss} [1]. In other words, once we measure device capacitances, we can guarantee the values of the gate charge parameters. The gate charge captures the charge needed to move the gate from 0V to the desired voltage, and integrates the non-linear capacitance over that voltage range.

The measurement of switching times are controlled by the following factors: [1,2]

- $t_{d(on)}$ – R_g, C_{iss}, V_{th}, g_m – relating to the device, and gate driver characteristics.
- t_{rise} – R_g, C_{rss}, C_{iss}, g_m, V_{th}, L_s - relating to the device, and gate driver characteristics, RL and circuit layout stray inductances
- $t_{d(off)}$ - R_g, C_{iss}, V_{th}, g_m – relating to the device, and gate driver characteristics.
- t_{fall} – R_g, C_{rss}, C_{iss}, g_m, V_{th}, L_s - relating to the device, and gate driver characteristics, RL and circuit layout stray inductances

Clearly, once the R_g, C_{iss}, C_{rss} for the device is measured, along with V_{th} and g_m in static testing, the switching parameters are automatically guaranteed for that device in a fixed switching circuit. The stray inductance of the packaged unit is not measured, but since it depends only on wire count and placement, the tight control of this parameter ensures very little variability in L_s.

Therefore, a measurement of R_g, C_{iss}, C_{rss} and C_{oss} is enough to guarantee the gate charge and switching time parameters for the device. Including the C_{oss}, this covers all device parameters that affect MOSFET switching losses.

Physics of dynamic parameters

A. Gate resistance

The distributed gate resistance of a power MOSFET is pictorially represented in figure 1. R_g is controlled by only a few factors for a device with a given layout

- Poly sheet resistance and width and thickness control
- Contact resistance between Gate metal and Poly
- Gate metal sheet resistance and width control
- Package gate wire resistance is usually a very small contributor to R_g, varies very little, and is ignored.

On each wafer, a long Poly Resistor is used to monitor the resistance of a line of Poly. A four terminal Kelvin measurement is performed on the structure located in the standard process control monitor (PCM) tested on each production wafer. R_{poly} behavior for typical AOS product is shown in figure 2.

The contact resistance between gate metal and Poly is monitored using a 4-terminal Kelvin structure. R_{gks} is monitored in the same fashion using the PCM. R_{gks} behavior for typical AOS product is shown in figure 3.

The metal sheet resistance for a 1000um long 10um wide metal bus is monitored using a structure located in the standard process control monitor (PCM) tested on each production wafer. R_{met} behavior for typical AOS product is shown in figure 4.

It is clear that control of these parameters is excellent in AOS products.

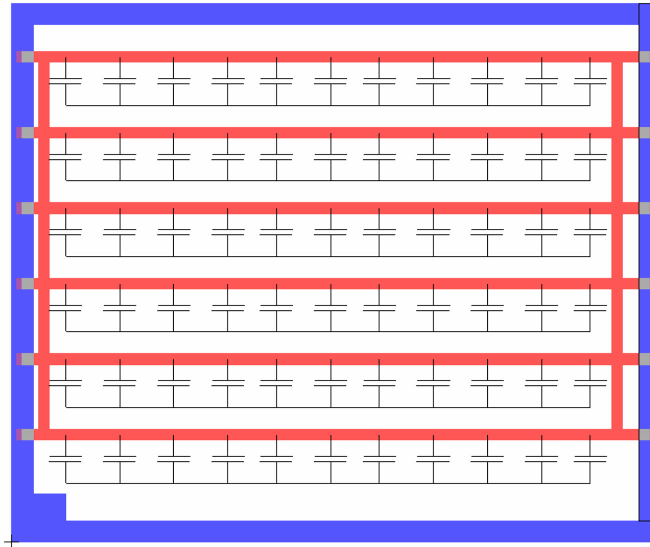

Figure 1: Model representation of the distributed gate resistance of a power MOSFET. The metal gate bus around the device is shown in blue. The gate pad is located at the corner in this case. Gate Polysilicon are shown in pink and they contact the metal bus at the edges of the die. The distributed capacitance between the gate Polysilicon and the silicon (Source/Drain) regions is represented by the capacitors distributed along the Gate.

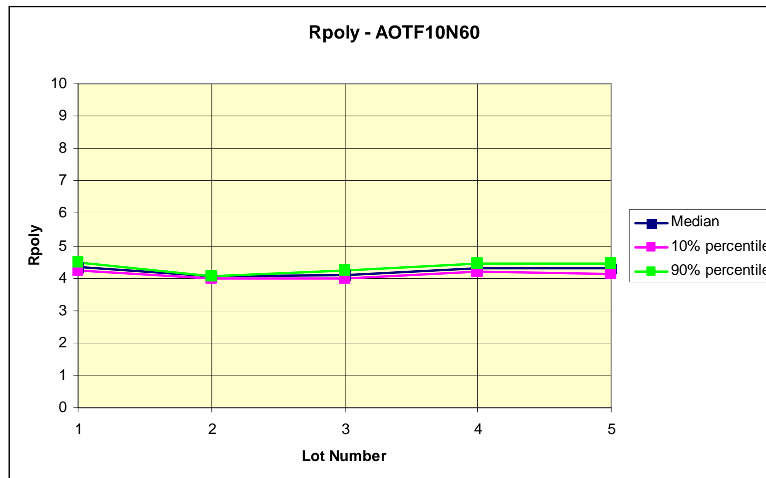

Figure 2: Poly resistance monitored for HV Planar MOSFET. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control. This plot covers a period from Jan - June 2008.

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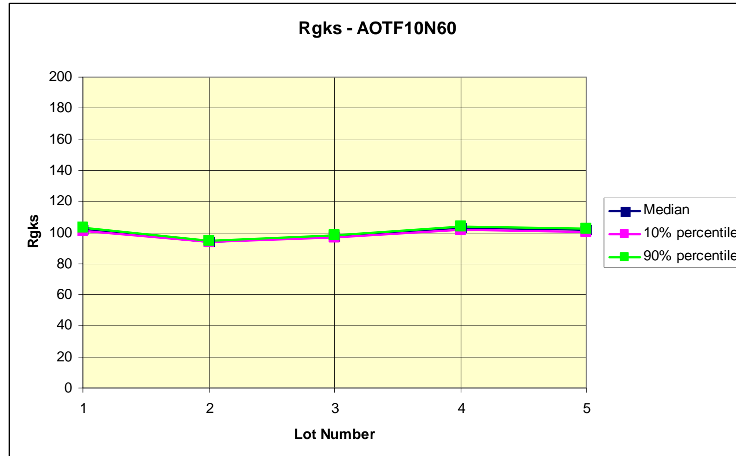

Figure 3: Gate contact resistance monitored for HV Planar MOSFET. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control. This plot covers a period from Jan - June 2008.

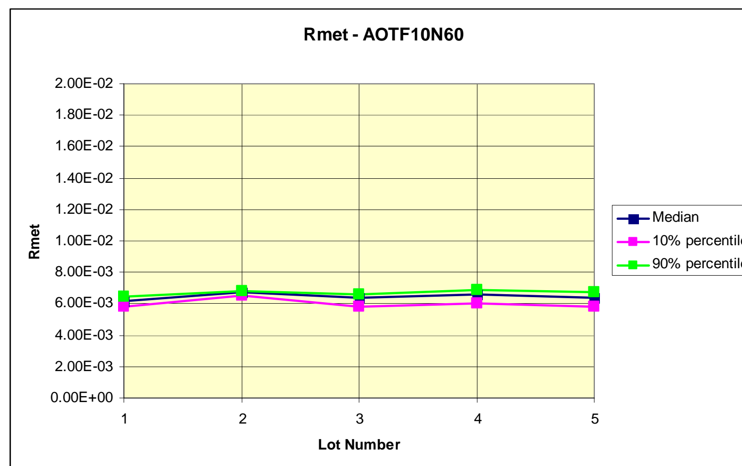

Figure 4: Resistance of a 1000um long 10um wide metal line monitored for HV Planar MOSFE. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control over metal resistivity, line width and film thickness. This plot covers a period from Jan - June 2008.

Now consider the distributed nature of the MOSFET R_g as shown in figure 1. If any one contact is not completely open, or a small area has a high R_{poly}, it will have little or no effect on R_g or the device, because the gate signal will re-route itself through the many parallel paths in close proximity. All AOS layouts are done with this in mind.

If the entire device has a problem with R_{poly}, R_{met} or R_{gks}, it can occur only if the wafer, or a section of the wafer has a problem with that parameter. By locating PCMs at the center and wafer edges, much of this can be monitored.

Measurement of R_g at the wafer level has traditionally been thought to be quite difficult for power MOSFETs designed for low R_g. This is true, so testing is often done 100% at the Final test station using one of the handler sites by AOS. Moreover, AOS has developed proprietary techniques to accurately test R_g of our devices at the wafer level, and simultaneously test the biased Ciss, C_{rss}, C_{oss} and static parameters. This technique is applied to a 200 site sample on the wafer to guarantee 100% R_g, Ciss, C_{rss} and C_{oss} parameters on the datasheet. Rg is also 100% tested at Final test to ensure goot gate wire contact to the gate pad. By extension, the gate charge and switching time parameters are 100% guaranteed.

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Figure 5 shows typical distribution of R_g on a wafer. Figure 6 shows a typical wafer map. Most of the variation in R_g, though small, is actually known to come for limitations of the tester. Figure 7 compares the test results between wafer probing and packaged device testing for the same device.

Figure 8 shows the lot to lot variation over time in the form of a control chart a typical high volume AOS products. Most of the guardband in R_g specification is applied to handle test capability issues and not due to actual wafer process capability.

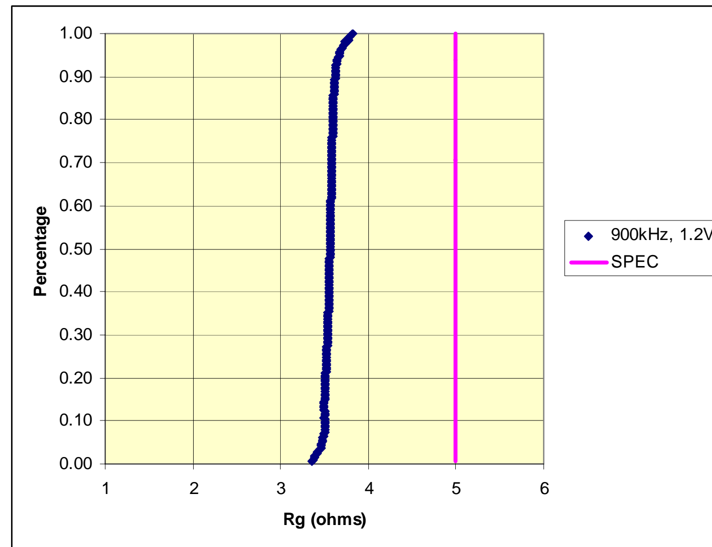

Figure 5: R_g distribution for 200 sites on a wafer taken on a HV Planar FET.

RG (Ohm)
Sum X

Y	4	6	8	10	12	15	18	20	23	26	29	32	34	37	40	42	44	46	48
3								3.8	3.7	3.7	3.8	3.7							
5						3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.7					
7					3.6	3.6	3.5	3.6	3.5	3.5	3.6	3.5	3.6	3.5	3.7				
9				3.5	3.5	3.5	3.5	3.5	3.5	3.6	3.6	3.6	3.6	3.5	3.6	3.7			
11			3.6	3.5	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.7	3.8		
14		3.5	3.5	3.5	3.6	3.6	3.6	3.6	3.5	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.6	
17		3.6	3.5	3.6	3.6	3.6	3.6	3.6	3.5	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.6	3.5	
20		3.5	3.5	3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.5	
23	3.6	3.5	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.5	3.7
26	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.8
29		3.5	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.6	3.5	3.6	3.6	3.6	3.6	3.5	3.5	3.7	
32			3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.6	3.6	3.6	3.6	3.5	3.5		
35			3.5	3.5	3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.6	3.6	3.6	3.6	3.5			
38					3.6	3.6	3.6	3.6	3.6	3.5	3.5	3.6	3.6	3.6	3.6				
40						3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6					
42							3.6	3.8	3.5	3.6	3.5	3.7							

Figure 6: Typical Wafer Map of Rg distribution. Probed column and row numbers shown in bold italics. Actual values shown on the wafermap. The values are very tightly distributed.

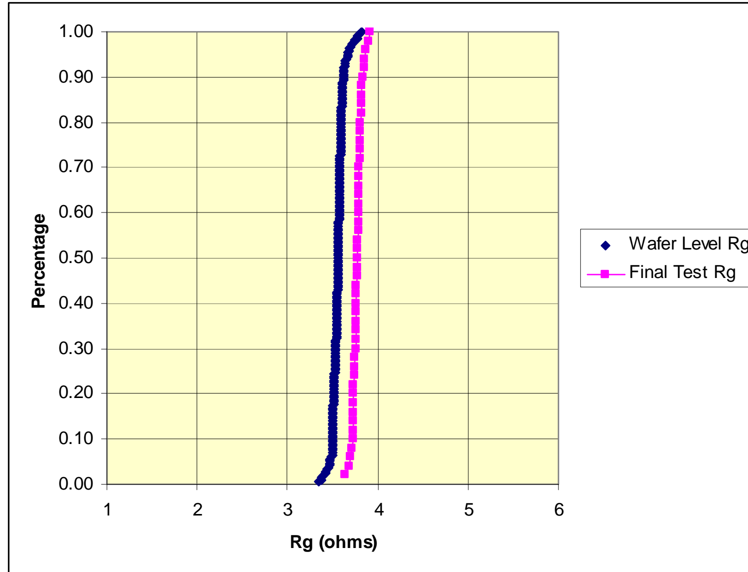

Figure 7: Comparison of wafer level and package level Rg measurements. Excellent agreement is obtained.

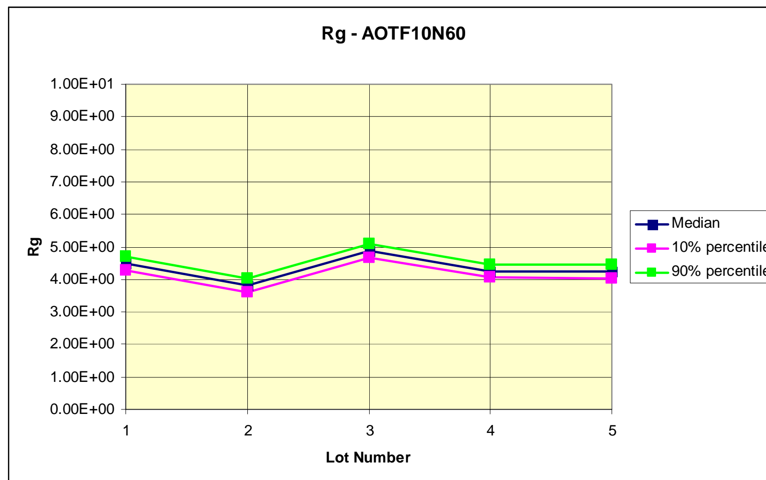

Figure 8: Lot by Lot trench chart of RG for a HV Planar MOSFET AOTF10N60. Note the tight 10th to 90th percentile lines, grouped right near the median line. Most of the variation is actually from test accuracy.

Device Capacitances

The datasheet capacitances are defined in terms of the structural capacitances as follows:

$C_{iss} = C_{gs} + C_{gd}$

$C_{rss} = C_{gd}$

$C_{oss} = C_{gd} + C_{ds}$

The C_{iss} for a Planar MOSFET is determined by

- layout parameters like Poly width, Cell pitch
- gate oxide thickness and uniformity
- Source-Body-Epi doping profiles
- Gate Poly doping is usually not a factor, since it is degenerately doped

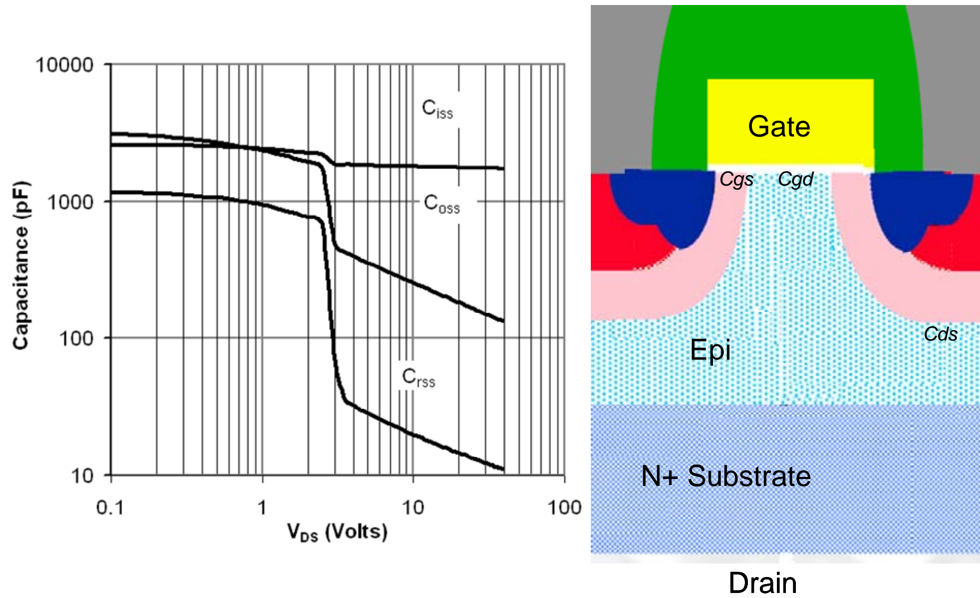

Figure 9: Device capacitances of the basic HV Planar power MOSFET.

This parameter is dominated by the capacitance between the gate Poly and the source-channel regions, which is not bias sensitive and very repeatable.

The C_{rss} for a HV Planar MOSFET is determined by

- layout parameters like Poly width, cell pitch
- gate oxide thickness and uniformity
- Body lateral diffusion, which determines the width of the "JFET" region
- Body-Epi and JFET region doping profiles
- Gate Poly doping is usually not a factor, since it is degenerately doped

This parameter is dominated by the width of the "JFET" region, JFET profile and epi doping profile.

The C_{oss} for a HV Planar MOSFET is determined by

- All parameters that affect C_{rss}, since it is part of C_{oss} and
- Body diode p-n junction area and doping profile

Figure 10 shows the typical distribution for these parameters on a wafer. Figure 11 shows the wafer map for the same distribution.

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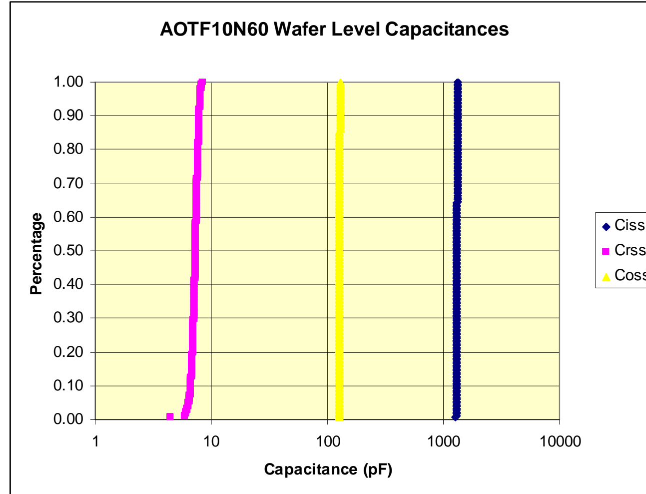

Figure 10: Distribution of Ciss, Crss, Coss for the 200 sites tested on a wafer (AOTF10N60). Excellent process control leads to a very tight parameter distribution.

CISS (pF)
Sum c X

Y	0	1	2	3	4	5	6	7	8	9	10	11
3					1320	1320		1330	1310			
4				1320	1320	1330	1330	1330	1330	1330		
5			1320	1320	1320	1330	1330	1330	1320	1330		
6			1320	1320	1320	1330	1330	1330	1320	1330	1320	
7		1310	1320	1320	1320	1320	1320	1330	1320	1320	1320	
8		1310	1320	1320	1320	1320	1320	1320	1320	1320	1320	1320
9		1310	1320	1320	1320	1320	1320	1320	1310	1320	1320	1320
10		1310	1320	1310	1320	1320	1320	1320	1320	1320	1320	1310
11		1310	1310	1320	1320	1320	1320	1320	1310	1310	1320	1310
12	1300	1310	1320	1310	1320	1320	1320	1320	1310	1310	1320	1310
13	1300	1310	1320	1310	1320	1320	1320	1320	1310	1310	1320	1310
14		1310	1320	1310	1310	1320	1320	1320	1310	1310	1320	1310
15		1310	1320	1310	1520	1320	1320	1320	1310	1310	1310	1320
16		1310	1320	1310	1310	1320	1320	1320	1310	1310	1320	1310
17		1310	1320	1320	1310	1320	1320	1320	1310	1320	1320	
18		1310	1320	1320	1310	1310	1320	1320	1320	1320	1320	
19			1320	1320	1320	1320	1320	1320	1310	1320	1310	
20				1320	1320	1320	1320	1320	1320	1320		
21				1320	1320	1320	1320	1320	1320	1310		
22					1320	1320	1320	1320	1310			

Figure 11: Wafermap of C_{iss} data showing the tight distribution of C_{iss} across the wafer.

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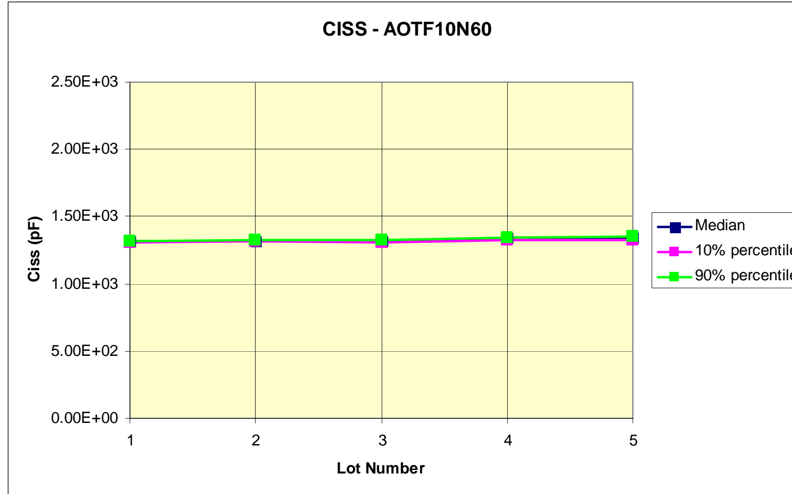

Figure 12: Lot to Lot variation in C_{iss} for AOTF10N60. Note the tight 10th to 90th percentile lines, grouped right near the median line.

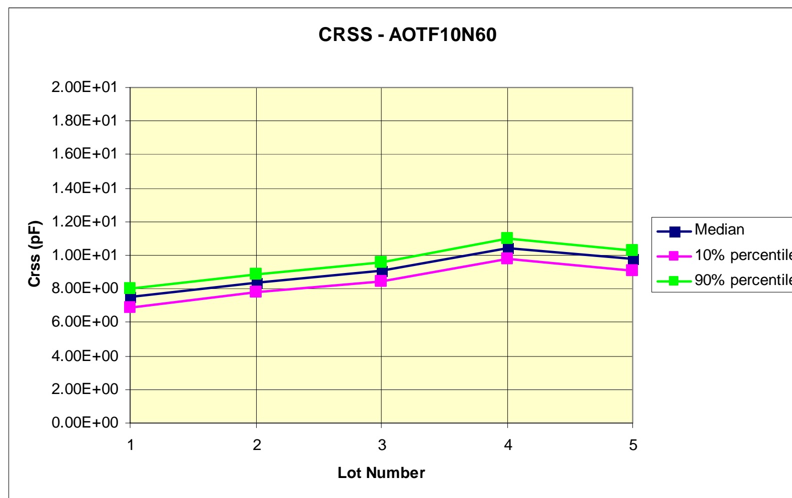

Figure 13: Lot to Lot variation in C_{rss} for AOTF10N60. Note the tight 10th to 90th percentile lines, grouped right near the median line.

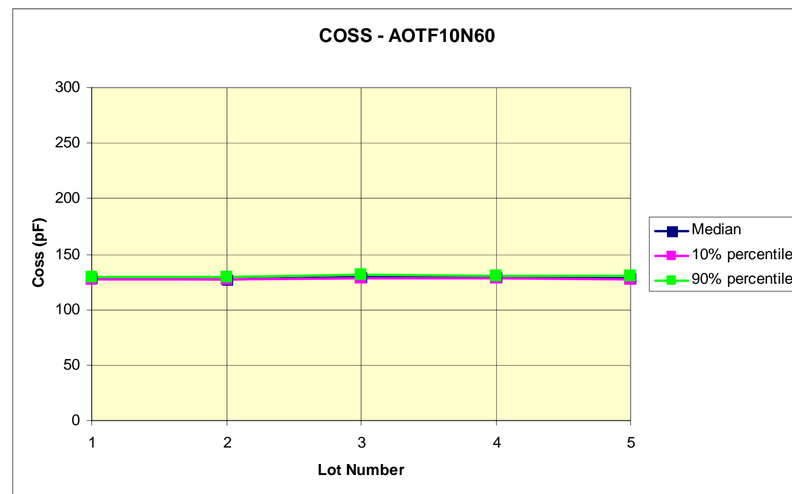

Figure 14: Lot to Lot variation in C_{oss} for AOTF10N60. Note the tight 10th to 90th percentile lines, grouped right near the median line.

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Figures 12, 13 and 14 show the lot to lot variation for a typical product. Note the tight control over the process this demonstrates.

The subtle changes in these capacitances together with the static parameter data for BV_{DSS}, R_{ds} and wafer map patterns help to determine whether incoming material, or process control factor is at work influencing the AC parameters, and provides a powerful tool for continuous improvement.

Conclusion

We have shown how a wafer level sample measurement of the MOSFET parameters R_g, C_{rss}, C_{iss} and C_{oss} is sufficient to 100% guarantee all the switching parameters of the device. (Q_{gs}, Q_{gd}, Q_g, $t_{d(on)}$, t_{rise}, $t_{d(off)}$, t_{fall}). Extensive measurements are used to show the accuracy and effectiveness of this wafer level testing scheme. Trend charts of both process level structural parameters, and actual measurements of R_g and capacitances are both shown. Excellent process control is shown to lead to excellent control over R_g and device capacitances for AOS MOSFETs.

Appendix I: Glossary of Terms

Q_g: Total gate charge to bring the MOSFET from V_{gs}=0V to a specified final value, e.g. 10V.
Q_{gs}: Gate-source charge. Portion of Q_g needed to charge the gate to its plateau voltage.
Q_{gd}: Portion of Q_g during which the Miller capacitance is charged.
R_g: Equivalent Series Resistance or Gate resistance of the MOSFET, measured between gate and source.
C_{iss}: Input capacitance at the gate.
C_{rss}: Reverse transfer capacitance.
C_{oss}: Output capacitance at the Drain.
V_{th}: MOSFET threshold voltage
g_m: transconductance
$t_{d(on)}$: turn on delay time
t_{rise}: Turn on current rise time
$t_{d(off)}$: turn off delay time
t_{fall}: turn of current fall time
L_s: Source Inductance

REFERENCES

[1] Modern Power Devices, B.J. Baliga, John Wiley and Sons, 1987.
[2] Power MOSFETs: Theory and Applications, D.A. Grant and J. Gowar, John Wiley and Sons, 1989.

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