A 1.12 pJ/b Inductive Transceiver With a Fault-Tolerant Network Switch for Multi-Layer Wearable Body Area Network Applications

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***Abstract*—A near-field coupling transceiver integrated with a fault-tolerant network switch is implemented for inter-layer and intra-layer Wearable Body Area Network. The inductive coupling transceiver employs a Resonance Compensator (RC) with a digitally controlled on-chip capacitor bank and a variable hysteresis Schmitt Trigger to compensate dynamic and static variances of woven inductor, and it enables 10 Mbps wireless transaction with the reception energy of 1.12 pJ/b at 2.5 V supply. The network switch introduces new fault-tolerant protocol to eliminate the routing table and reduces power consumption by 70% compared with the conventional switch using torus topology. The transceiver with the switch and the RC are implemented in 0.25-μm 1P5M CMOS process technology, occupying 2.0 mm^2 and 0.8 mm^2 area, respectively.**

***Index Terms*—Capacitor bank, digital compensation, fault tolerance, fault-tolerant network, inductive coupling, resonance compensation, wearable network.**

I. Introduction

RECENTLY, Body Area Network (BAN), or wearable network is becoming important to implement personal healthcare systems and mobile entertainment systems [1]. There are two approaches to form a BAN; one uses wireless communication, and the other uses wireline. For wireless technologies, ZigBee, Bluetooth, and Wireless LAN (WLAN) are used. However, these wireless-based technologies suffer from interference, fading, and low data rates [2]. In addition, they are not suitable for healthcare applications where inelastic data transmission must be guaranteed for "always reliable" communication. Especially, ZigBee and Bluetooth are vulnerable to interferences at 2.4 GHz [3], because they share the same frequency range with WLAN, so that they have difficulty in communication under WLAN environments [4], [5]. In addition, Bluetooth is influenced significantly by requirement to establish the line-of-sight (LoS) [6]; when reflection is absent such as in open area, the LoS requirement becomes more stringent, because human body plays as an obstacle for 2.4 GHz signals. Therefore, considering the "always reliable" requirements of healthcare applications, ZigBee and Bluetooth are not sufficient.

As an alternative to the wireless approaches, wireline-based technologies are introduced to meet the BAN requirements. Integrating the communication network into clothes to form a wireline Wearable Body Area Network has been tried for healthcare or multimedia applications [7]–[10], using conducting thread as their interconnection material. However, wearable network has 4 unique networking situations that must be considered: first, since clothes are multilayered, such as underwear, inner wear, and outer wear, low power wireless links are necessary to couple the multilayered clothes. Second, since 2-D network structure is embedded in 3-D clothes space, its 3-D clothes shape changes over time and with gesture (dynamic deformation). Third, knitting and weaving are not electrically exact technologies, and their properties are too irregular to achieve an efficient communication (static parameter variation). Therefore, electrical compensation for the inaccuracy is required. Finally, fabric in nature is prone to tearing and wearing out, thus the wearable network must be tolerant to faults.

Several works have shown the concept and implementations of wearable network; a novel concept of Fabric Area Network (FAN) was introduced in [8], but the size of antenna was bulky and the data rate ($<$125 kbps) was low. A breakthrough fault-tolerant wearable network was shown in [9], [10], but the work was limited to intra-layer (within a layer) network, and there was no chip implementation to integrate on. Moreover, [9], [10] used torus topology, which requires continuous monitoring of link faults even if there is no data transaction, resulting in waste of energy. For wireless proximity communication, efficient board-to-board [7], novel low-energy chip-to-chip [12]–[14], and short-distance planar sensor-to-sensor [15] transceivers were proposed. Since these transceivers are designed to deal with static environment such as on-chip or on-board inductors, they are not optimized for wearable networks where dynamic and static variances are non-negligible.

Although these previous works showed the concept of wearable network and fault-tolerance, or proximity communication transceivers, no low-power CMOS chip has been implemented to provide both inter-layer (between layers; wireless) and intra-layer (within a layer; wireline) communication at the same time,

Manuscript received February 06, 2009; revised April 24, 2009. Current version published October 23, 2009. This paper was approved by Guest Editors Hoi-Jun Yoo and SeongHwan Cho.

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Digital Object Identifier 10.1109/JSSC.2009.2028952

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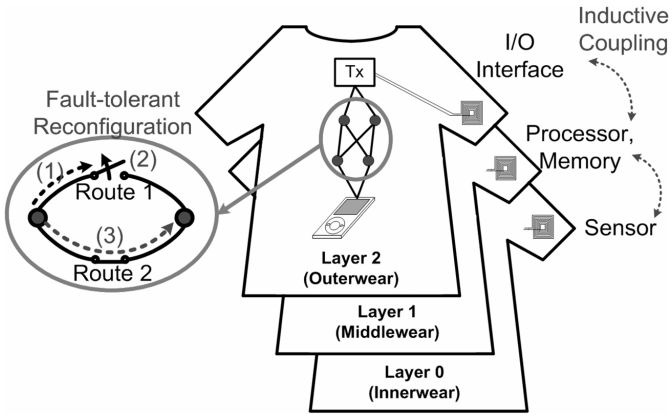

Fig. 1. Proposed wearable network concept.

nor have practical network protocol and digital compensation of resonance frequency for wearable networks been made yet.

This paper presents a CMOS-based digitally compensated inter-clothes near-field coupling transceiver, integrated with an intra-clothes network switch that realizes the fault-tolerant network protocol and energy efficient wearable networks. Fig. 1 shows the concept of the proposed wearable network [16]. Multiple layers are connected by inductive coupling link, and each layer has its own function, such as I/O interface, processor, memory, or sensor. In addition, within a layer, fault-tolerant network scheme is introduced so as to reconfigure its route in case of faults.

Fig. 2 is the system architecture of the proposed wearable network system implemented in two separate chips. It is composed of an inductive transceiver, a resonance compensator, a 5×5 switch, and a Power Management Unit (PMU). The inductive transceiver provides inter-layer (wireless) communication link, with the woven inductors made out of conductive yarn; it exploits a variable hysteresis Schmitt Trigger to deal with static variations of the woven inductors. The Resonance Compensator (RC) cooperates with the inductive transceiver to periodically compensate dynamic deformation of woven inductors. The 5×5 switch provides intra-layer (wireline) communication link, and it automatically re-routes the link when fault is found, to incorporate fault-tolerance. The transceiver and the switch share the packet generator and the payload recovery block. Finally, the PMU controls the four different power and clock domains [Switch (SW), Transmitter (TX), Receiver (RX) and Resonance Compensator (RC)], based on operation modes to reduce overall power consumption.

This paper is organized as follows. Section II describes design considerations of woven inductor with conductive fabric wires. In Section III, design of a resonance compensated inductive transceiver for inter-layer communication is described in detail. Section IV presents a fault-tolerant network switch for intra-layer communication. Implementation results will follow in Section V, and finally, Section VI concludes the paper.

II. Woven Inductor Design

In wearable network environment, the proximity between the layers introduces near-field coupling as a strong candidate to form an inter-layer link. Conventional inductive coupling approaches [12]–[14] have shown good performance under chip-to-chip environments, but the communication range (<50 μm) is too short because of the small on-chip inductor, and they are not suitable for wearable network. Communication range can be extended by using larger inductors [17], but this approach uses rigid on-board inductor and hence, is not a good option for wearable environment. Therefore, we propose woven inductors that are made out of conductive yarn. It is woven into cloth to form an inductor, so wearability, flexibility, comfort and ease of manufacturing are achieved at once. Moreover, the woven inductor shows large enough inductance ($\sim\mu$H), so it is suitable for wearable environment where up to cm-range near-field communication is required. However, the flexibility leads to change in link gain between two inductors; thus proper compensation is required, and details of the compensation method are described in Section III.

Fig. 3 shows an example of a woven inductor on a cloth. It is made out of the conductive yarn, which is composed of seven 10-to-20 μm copper warp thread. The fluorine resin coating surrounds the warp thread for protection and more mechanical strength. This conductive yarn shows about the same mechanical strength and flexibility as typical cotton thread, and we can easily weave or knit it on cloth. We use an 8-turn woven inductor with 1.5 cm diameter that has inductance measured as 2.5 μH, and its self-resonance frequency of around 30 MHz with $\mathrm{Q} = 15$.

Fig. 4(a) shows the deformation parameters of a woven inductive link. The gain of an inductive link is defined as the ratio between peak voltages of TX and RX inductors when a pulse is applied to the TX inductor; the gain of the inductive link is measured in terms of misalignments along x, y and z axes [Fig. 4(b)]. The measurement shows dynamic deformation varies its inductance value by up to 45%. On the other hand, static variance due to large inaccuracy of the sewing or weaving is measured as 17% among 30 woven inductors [Fig. 4(c)]. From the measurement, the following equation is drawn for link gain:

$$\mathrm{Gain}_{\mathrm{Link}} = k \cdot \frac{A_{\mathrm{cross}}^2 \times N_{\mathrm{RX}}}{d \times A_{\mathrm{TX}} \times N_{\mathrm{TX}}} \tag{1}$$

where k is the constant (which is measured to be 0.00342), A_{cross} is the cross section area between two inductors, A_{TX} is the area of TX inductor, N_{TX} is the number of TX inductor turns, N_{RX} is the number of RX inductor turns and d is the distance between two inductors. A_{cross} can be induced from

$$A_{\mathrm{cross}} = x_{\mathrm{cross}} \cdot y_{\mathrm{cross}} \tag{2}$$

where x_{cross} and y_{cross} are defined as in Table I. For example, if diameter of a TX inductor (x_{TX}) is the same with the diameter of the RX inductor (x_{RX}), and the misalignment between TX inductor and RX inductor with respect to x and y axes are Δx and Δy respectively, then x_{cross} is equal to $\mathrm{Min}(x_{\mathrm{TX}}, x_{\mathrm{RX}}) -$

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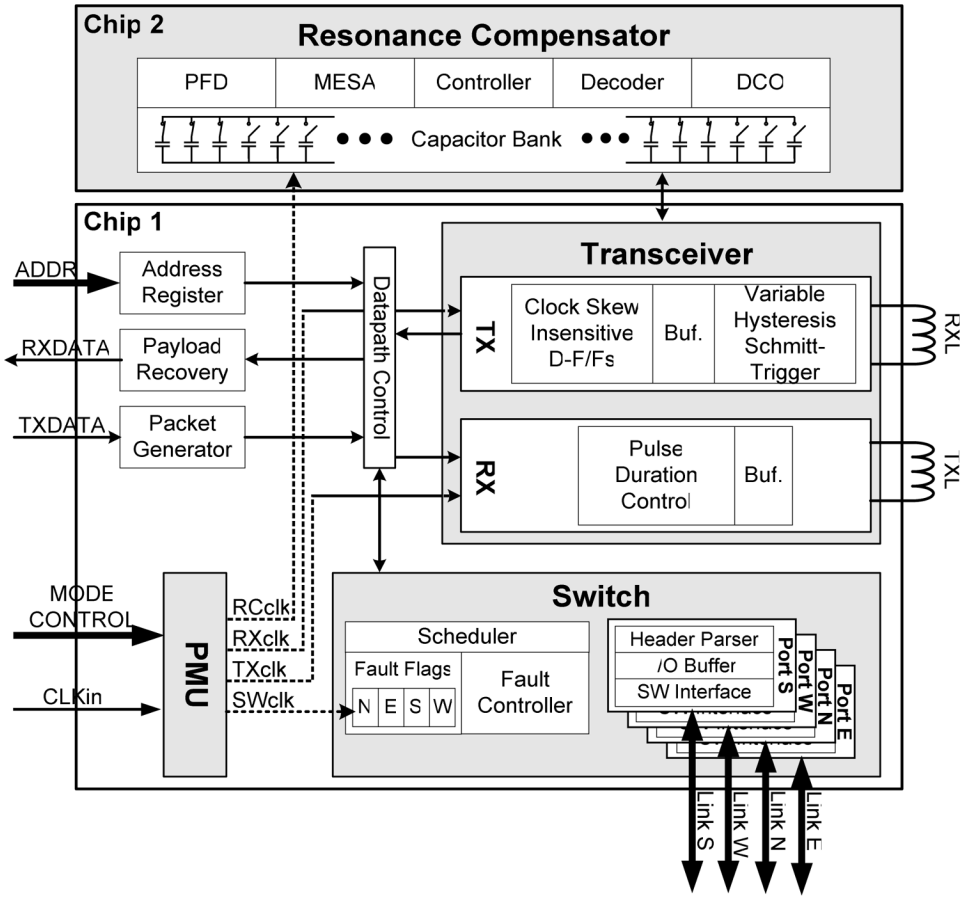

Fig. 2. System architecture of the proposed wearable network system implemented in two chips.

TABLE I
DEFINITIONS OF $x_{\rm cross}$ AND $y_{\rm cross}$

Condition	x_{cross}	y_{cross}
$\lvert x_{TX} - x_{RX} \rvert > \Delta x$	$\min(x_{TX}, x_{RX})$	-
$\lvert x_{TX} - x_{RX} \rvert \le \Delta x$	$\min(x_{TX}, x_{RX}) - \Delta x$	-
$\lvert y_{TX} - y_{RX} \rvert > \Delta y$	-	$\min(y_{TX}, y_{RX})$
$\lvert y_{TX} - y_{RX} \rvert \le \Delta y$	-	$\min(y_{TX}, y_{RX}) - \Delta y$

x_{TX}, x_{RX}: width of TX and RX inductors
y_{TX} , y_{RX}: height of TX and RX inductors

$\Delta x = x_{\rm TX} - \Delta x$. The same calculation leads to $y_{\rm cross} = y_{\rm TX} - \Delta y$. Putting these results into (2) and (1) leads to the link gain:

$$\mathrm{Gain}_{\rm link} = k \cdot \frac{(x_{\rm TX} - \Delta x)^2 \cdot (y_{\rm TX} - \Delta y)^2 \cdot N_{\rm RX}}{d \cdot x_{\rm TX}^2 \cdot N_{\rm TX}}. \quad (3)$$

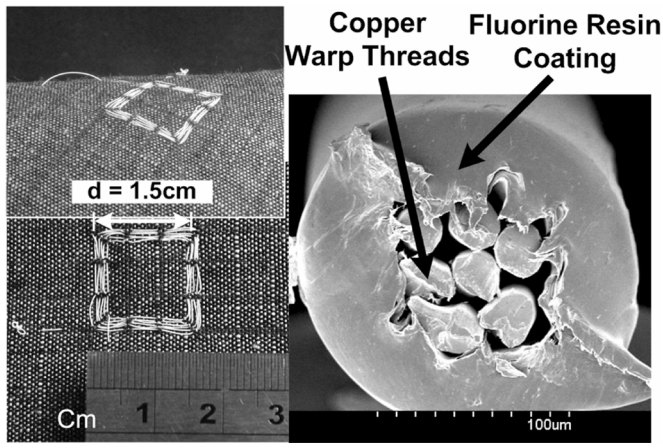

Fig. 3. Woven inductors in fabric, and the conductive yarn to form the inductors.

III. RESONANCE COMPENSATED INDUCTIVE TRANSCEIVER

A. Inductive Transceiver Design for Wireless Link

As described in Section II, wearable environment varies with respect to time and space. Therefore, the wireless inter-layer communication in wearable network must deal with these dynamic and static variances. Also, due to the strict battery constraints of wearable environment, low power operation is essential. As a solution, we propose the inductive transceiver with a variable hysteresis Schmitt Trigger to compensate the static variances (Section III-A). Also, the Resonance Compensator (RC) is described in detail (Section III-B), to effectively compensate the inaccuracies and variances caused by dynamic deformation of woven inductive link. As a result, the proposed transceiver achieves low power operation, while effectively

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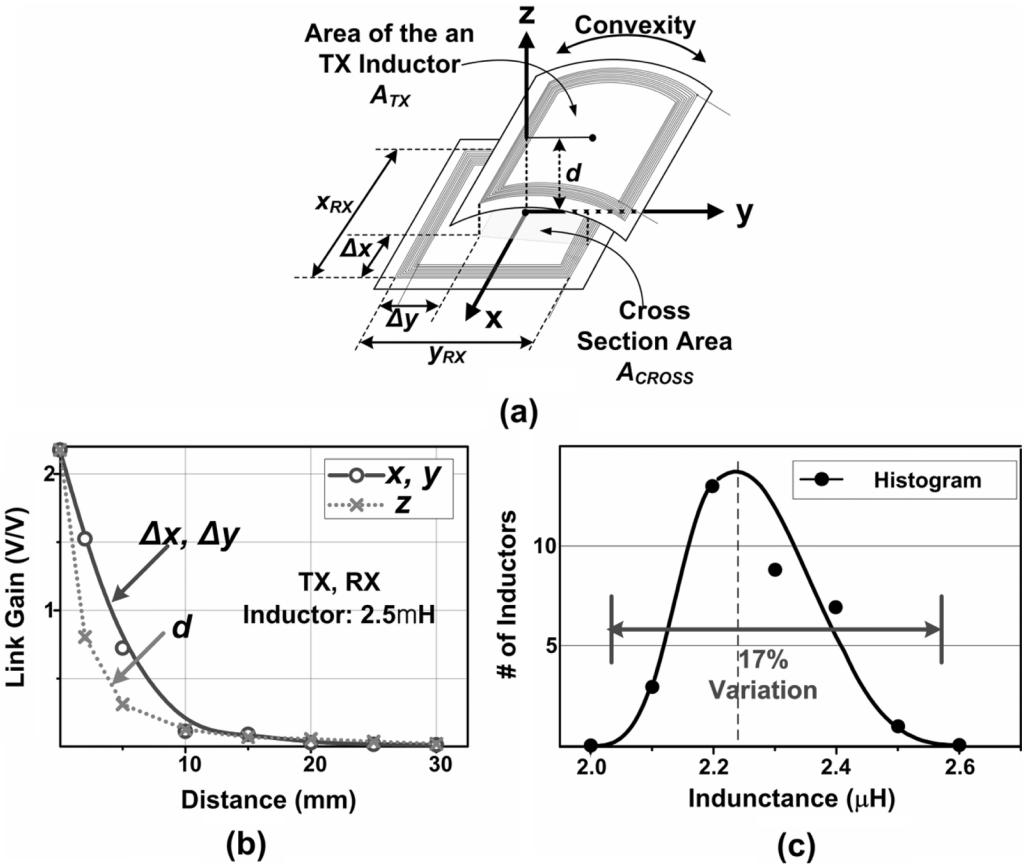

Fig. 4. (a) Deformation parameters, (b) link gain versus alignment, and (c) static variance of woven inductors.

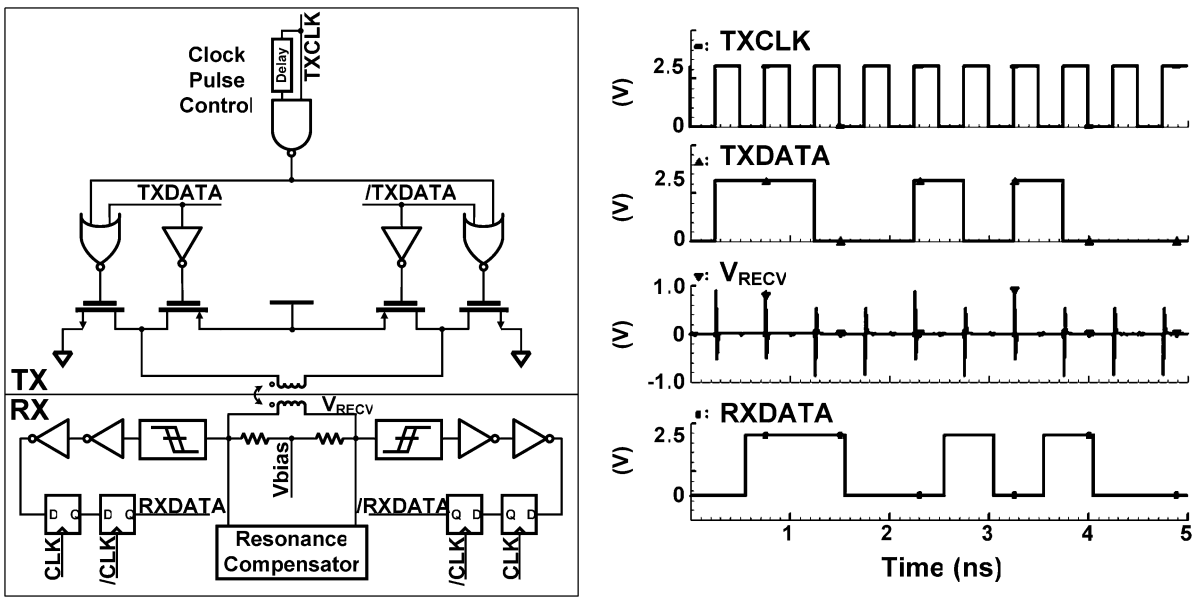

Fig. 5. Inductive transceiver and its simulation results.

compensating the static and dynamic variances of a woven inductor link.

Figs. 5 and 6 depict the resonance compensated inductive coupling transceiver and its application block diagram, respectively. The biphase modulation (BPM) inductive transmitter [12], [13] is adopted in transmitter, and the TX uses pulse-based signaling with duration control. At every positive TX clock (TXCLK) edge, the H-bridge in transmitter generates positive and negative pulse current in the transmitting inductor for input TXDATA of "1" and "0", respectively. The pulse duration is determined by the delay in the clock pulse control. We take advantage of the BPM since it always generates $\mathrm{V_{RECV}}$ signal

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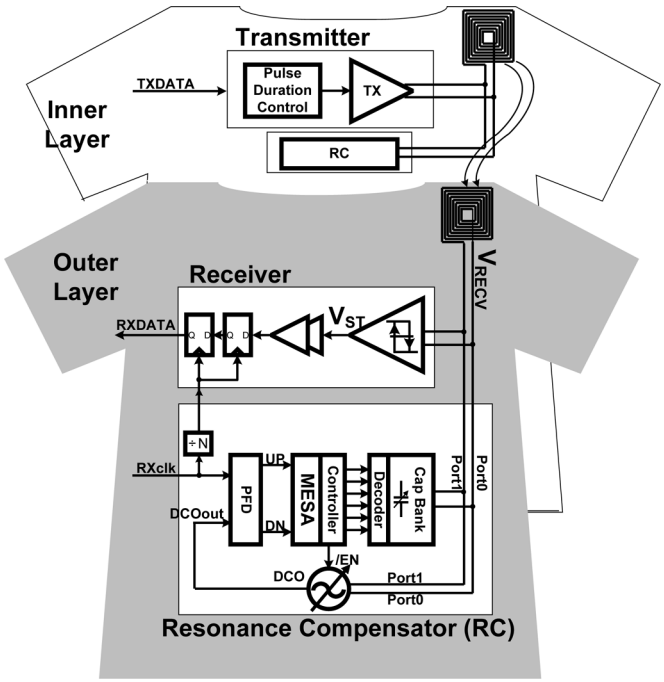

Fig. 6. Application block diagram of the proposed resonance compensated inductive transceiver.

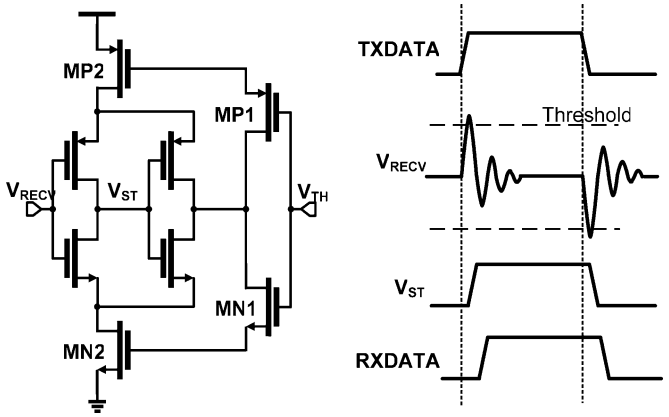

Fig. 7. Variable hysteresis Schmitt Trigger.

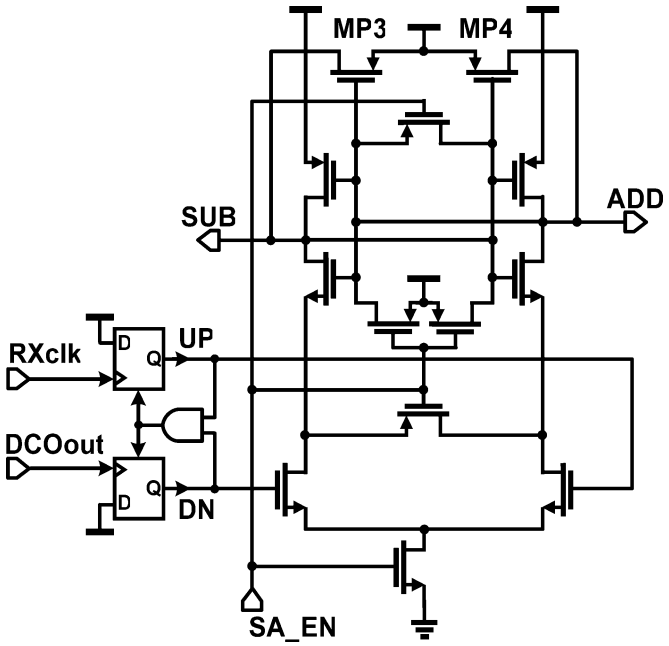

Fig. 8. Mutually exclusive sense amplifier (MESA) with the phase frequency detector (PFD).

at each TXCLK positive edge for better noise immunity [13]; conventional non-return-to-zero scheme generates V_{RECV} signal only when there is a TXDATA transition prior to positive TXCLK edge.

The RX is composed of a variable hysteresis Schmitt Trigger and the clock-skew insensitive C^2MOS D-flip-flops [11]. Because of the static variation of the woven inductor link, conventional near-field coupling receivers [12]–[14], [17] are not affordable. Static variation results in fluctuation in received signal strength, V_{RECV}, and the logic threshold change is necessary to detect "0" and "1" under this fluctuation between inductors; we adopt the variable hysteresis Schmitt Trigger to do so. Fig. 7 shows the variable hysteresis Schmitt Trigger. The logic threshold of Schmitt Trigger is set by the other input, V_{TH}, and it determines the feedback amount through MP1 and MN2. For low energy operation, short circuit is prevented by MP2 and MN2, eliminating additional sense-amps or sampling timing control circuits. Simulation results (Fig. 5) show that with 2.5 μH inductors, TXDATA is successfully recovered through the receiver as RXDATA.

B. Resonance Compensator (RC) Design

In addition to the large inaccuracy of the sewing or weaving, woven inductors are easily deformed so that the value of inductor is time- and space-variant. To compensate this dynamic variation, the RC of Fig. 6 is adopted with digitally controlled capacitor bank. Conventional frequency control method [18] uses charge-pump and ADC, but the RC removes them so that it only consumes 0.17 mW when active.

In the proposed RC, a capacitor bank and a woven inductor form a *LC* tank; when inductor is dynamically deformed, the resonance frequency of the *LC* tank is shifted, and therefore, the RC can detect this offset through the phase frequency detector (PFD) and mutually exclusive sense amplifier (MESA) by comparing the resonance frequency with the reference clock (Fig. 8). The offset is then compensated through decoder by adjusting the number of on-capacitors in capacitor bank with ADD/SUB signals. The output of the PFD, either UP or DOWN, is fed to the RC controller through MESA. The MESA selects a signal which arrives earlier, and generates ADD (add more capacitors to decrease frequency), or SUB (vice versa) (Fig. 8). MP3 and MP4 provide positive feedback to strengthen the output signal. The decoder then shifts the oscillator frequency by switching the unit cells of capacitor bank on or off; in each cycle, the RC updates the amount of total unit cells turned on, by twice or by half when MESA output is ADD or SUB, respectively.

Fig. 9 shows the 32×32 capacitor bank architecture, each unit cell having 0.1 pF. As shown in Table II, each unit cell can be selected either by row or by individual cell, with 3 control

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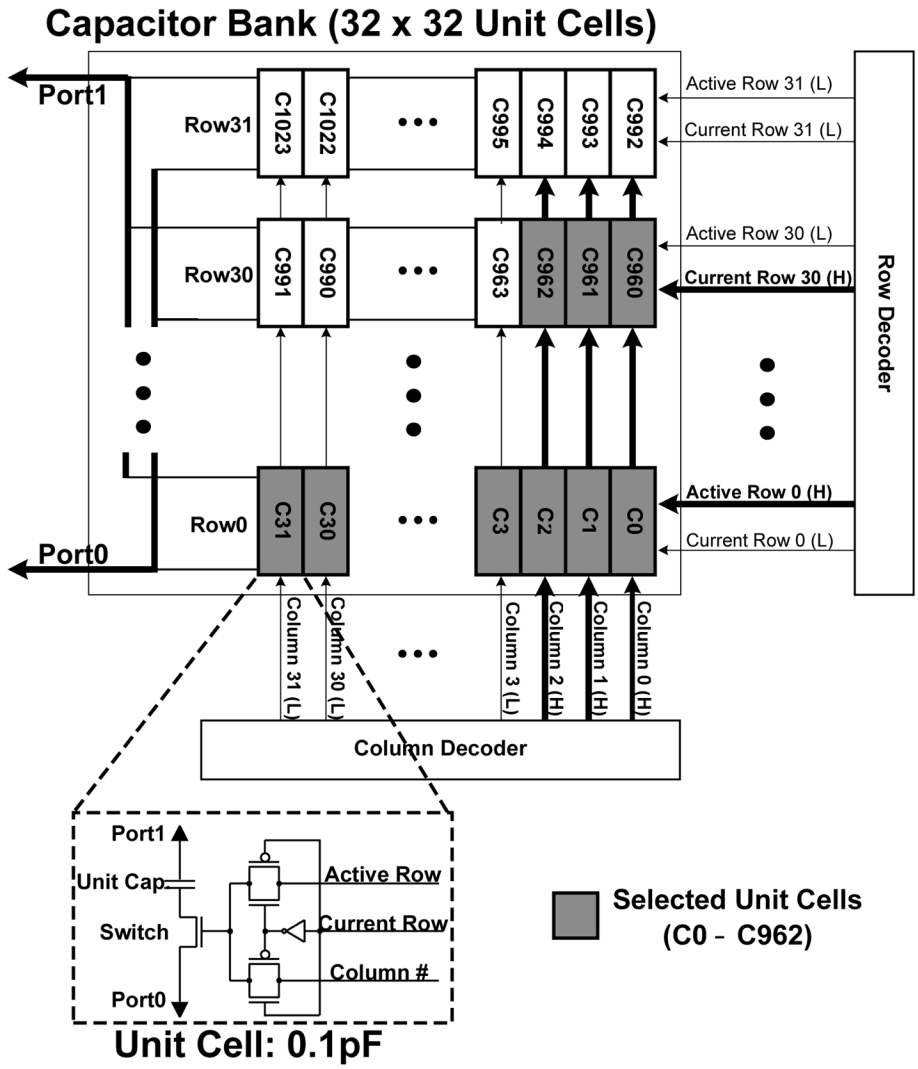

Fig. 9. Capacitor bank architecture with 32×32 unit cells.

signals generated from column and row decoders. If Active Row X is high and Current Row X is low, all of the capacitors in row X are turned on; on the other hand, if Active Row X is low and Current Row X and Column Y are high, then the unit capacitor at (X, Y) position is turned on. To calculate the overall capacitance of the selected capacitors, the following equation is used:

$$C_{\text{sel}} = \sum_{m} C_{\text{row}} + \sum_{n} C_{\text{unit}} = (32m + n) \cdot C_{\text{unit}} \tag{4}$$

where C_{sel} is overall capacitance of the selected capacitors, C_{unit} is unit capacitance, C_{row} is capacitance of a row, m is number of active rows and n is number of active column. For example, in Fig. 9 the capacitor banks in Active Row 0–29, Current Row 30, and Column 0–2 are all ON. In this case, the capacitance of selected capacitors will be $(32 \times 30 + 3) \cdot 0.1 = 96.3$ pF.

Fig. 10 is the decoder algorithm for capacitor bank. The compensation is done in binary fashion. The total capacitance of the bank is 102.4 pF, and combined with 20 pF offset capacitance, the RC can control the resonance frequency from 9.0 MHz to 22.5 MHz by 1024 steps with 3.7 kHz minimum step frequency for a 2.5 μH inductor. The resonance frequency f_R is given as follows:

$$f_R = \frac{1}{2\pi\sqrt{L \cdot (C_{\text{sel}} + C_{\text{offset}})}} \tag{5}$$

where C_{offset} is the offset capacitance of the digitally controlled oscillator (DCO) within the RC.

Fig. 11 shows the DCO. The woven inductor and the capacitor bank form an *LC* tank, and the resulting cross-coupled negative resistance amplifier oscillates at the resonance frequency. When the oscillator frequency gradually converges to the reference

TABLE II
CAPACITOR BANK OPERATIONS

Active Row X	Current Row X	Column Y	Turned ON Capacitors
High	Low	Don't Care	All caps in row "X"
Low	Low	Don't Care	-
Don't Care	High	High	Unit cap in (X, Y)

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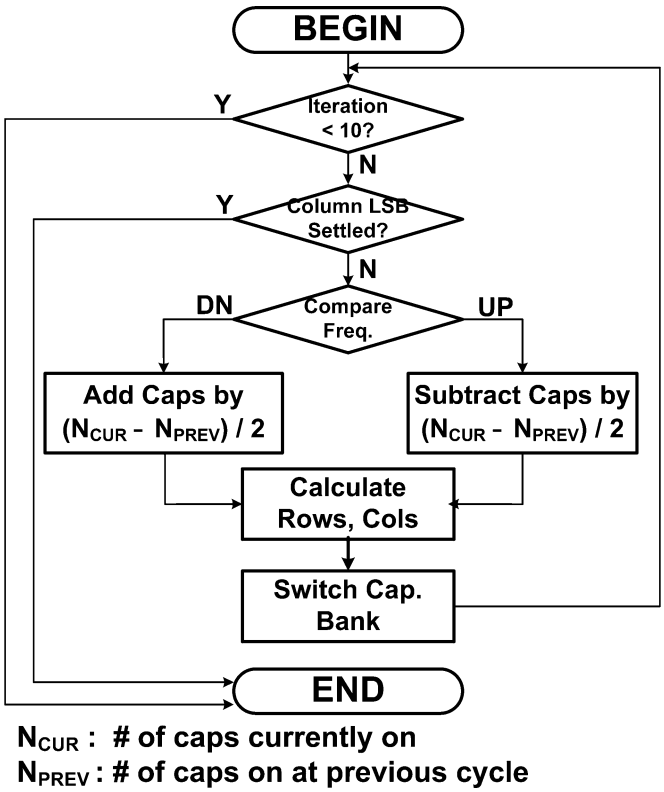

Fig. 10. Resonance compensator algorithm.

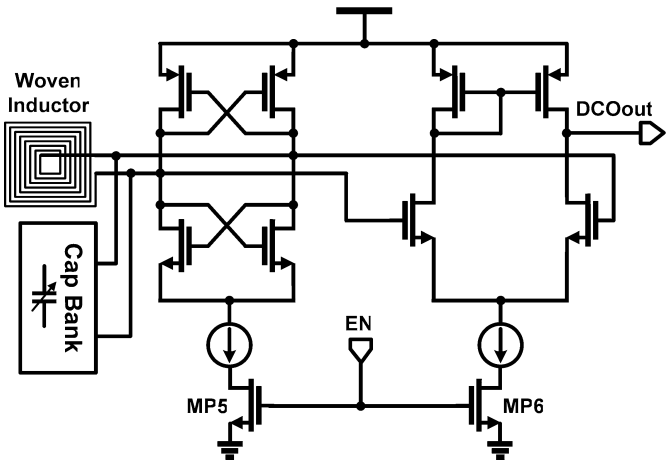

Fig. 11. Digitally controlled oscillator (DCO).

value in 10 iterations, the oscillator is cut off by MP5 and MP6 (in Fig. 11), and only capacitors are connected to the woven inductor. To further reduce energy consumption, the capacitor bank controller adaptively updates the compensation period. For example, if the bank value did not change for the last 3 trials, the compensation period is extended by twice, and if the value successively changed, use half the current period; otherwise, the same period is applied. The RC is implemented as a separate chip and is attached only to nodes that need inter-clothes communications.

IV. Fault Tolerant Network Switch

Harsh wearable environments such as washing, tearing, wearing or cutting make wearable network prone to faults. Yet the battery constraints limit the power consumption of wearable network. In addition, wearable network has prospective applications that include healthcare system or personal entertainment system, which have wide range of data rate [19]. Therefore, the proposed wearable network must provide fault tolerance with variable data rate.

The simplest method to make the network tolerant to faults is to have redundancy, that is, to have multiple buses between two nodes. Even if one or more bus is broken, the remaining buses will transmit data through them. This may be a good solution if there are plenty of wires and they are free from connection complexity. However, the wearable network with conductive yarns is exactly the opposite case; it is difficult to have multiple connections between nodes since it is difficult to connect chips on clothes with tens of wires on it. We should minimize the number of wire connection per chip for high manufacturability and low cost. Of course, we should still have fault-tolerance.

To provide fault-tolerance while keeping the number of wires per chip minimized, we choose 5×5 switch. Fig. 12 shows the architecture of the proposed wearable network and its packet structure. Conductive yarns composed of seven 10-to-20 μm copper warp threads are used to form a wearable network. The switch supports 3 different topology modes: tree, star and mesh. When most of the network traffics occur locally, the tree topology is utilized. Star topology is the most energy-efficient and can be applied when network fault is not a major issue. In contrast, mesh topology is the most robust to faults, and is appropriate to construct a BAN with wearable network.

The packet is designed to support multiple communication layers and has 3 components: a PHY header, a variable length payload, and a PHY footer. As shown in Fig. 12, the PHY header is made up of 4 fields; 4b sync, 12b length, 16b source address, and 16b destination address. A unique 16b address is assigned to each node to identify the current node's position: a 4b layer ID, a 4b section ID, and an 8b node ID which is composed of x- and y-addresses. A layer ID defines the current layer, and each layer is partitioned into sections. An example is shown in Fig. 12, and the right arm, front arm and left arm has section ID of 1, 2 and 3, respectively. To sum up, if a node have address of $0 \times$ x1221, the node is placed in layer 1, section 2, and $(\mathrm{x}, \mathrm{y}) = (2, 1)$. A flexible load size enables a packet to adapt to various data rate applications.

Before any routing begins in a switch for the first time, hybrid routing scheme verifies the link between the source and destination to search for faults. A switch has 4 links (ports) in 4 directions: North (N), South (S), East (E) and West (W). To obtain the fault-tolerance, hybrid routing scheme is split into 2 phases: fault search, and normal routing. During the fault search phase, as shown in the measured results in Fig. 13(a), the source (Node A) sends a request packet (REQ) toward destination (Node B), and an acknowledgment packet (ACK) back to the source means

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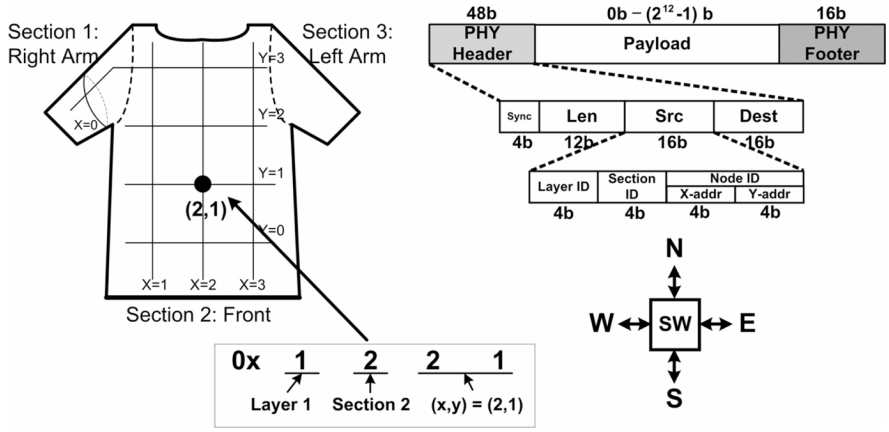

Fig. 12. Addressing strategy and the packet structure for the proposed wearable network.

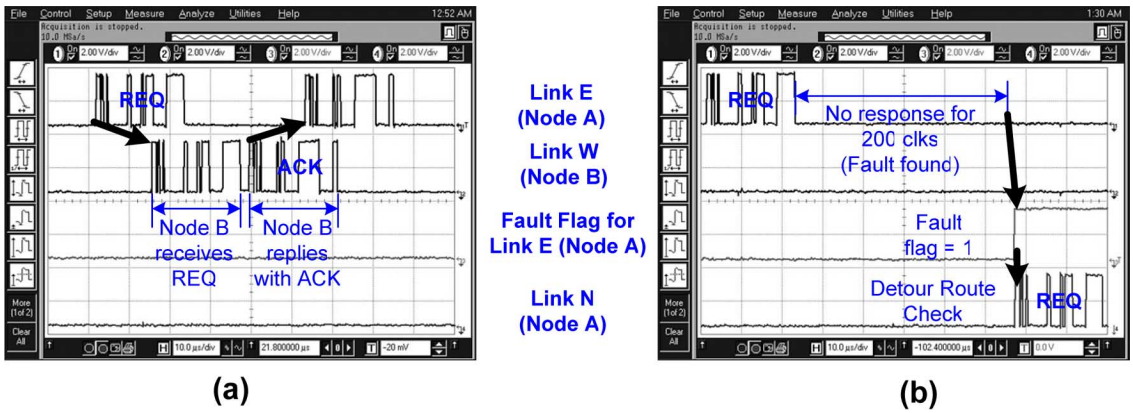

Fig. 13. Measured results of the hybrid routing for (a) no fault and (b) fault cases.

TABLE III
ROUTING RULES

NORMAL			FAULTY EAST & WEST LINKS		
X-Address	Y-Address	Link	X-Address	Y-Address	Link
D > C	Don't Care	E	Don't Care	D > C	N
D = C	D > C	N	D > C	D = C	N
	D = C	D. Reached	D = C		D. Reached
	D < C	S	D < C		N
D < C	Don't Care	W	Don't Care	D < C	S

D: Destination Address
C: Current Address

no-fault. Then the Node A, that sent the REQ, turns off the fault flag for link E, which means that the link E is clean without any fault. On the contrary, as in Fig. 13(b), if any switch along the path finds fault, no ACK will follow the REQ, and the Node A turn on the fault flag for link E.

Based on the destination address, current node's address, and fault flag, normal routing is performed. Since fault-finding phase is done only when the system is reset, continuous search for fault is unnecessary. The hybrid routing, combined with cut-through routing, removes unnecessary energy to search for faults and to find the destination address; measured results show that the proposed switch consumes 2.7 mW, and 70% power reduction is achieved over the scheme using torus topology with routing tables [9], [10].

Fig. 14(a) illustrates the concept of the proposed fault-tolerant routing. During the normal routing phase, cut-through routing is employed, and as soon as the switch parses the header to get the destination address, it routes the packet to an appropriate link, comparing x addresses first, and then y addresses without using routing tables. However, if the desired link is in fault, the switch routes by comparing y addresses first instead of x addresses. Table III shows the routing rules for the proposed switch. Measured waveforms of a switch [Fig. 14(c)] show a detour route is selected when fault is present in the case of Fig. 14(b).

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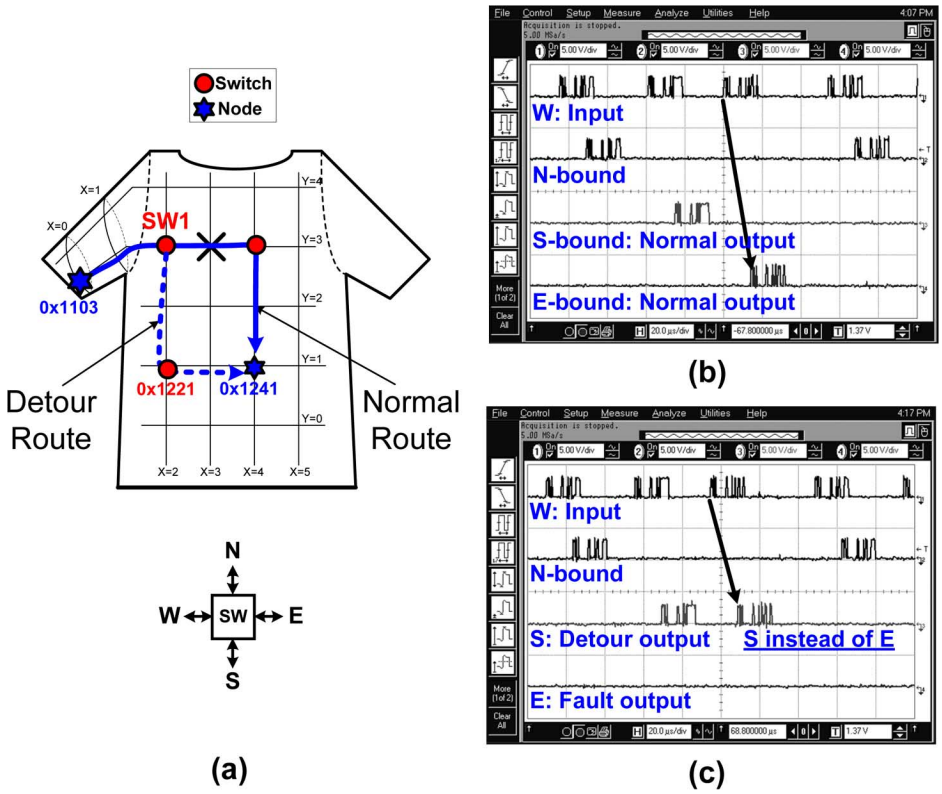

Fig. 14. (a) Fault-tolerant routing and the measurement results for (b) non-fault and (c) fault cases.

TABLE IV
PERFORMANCE SUMMARY

Technology		0.25μm 1P5M CMOS
Data Rate		~ 10Mbps
Routing Method		Cut-Through
Reception Energy		1.12pJ/b
Supply Voltage		Core 2.5V, I/O 3.3V
Power Consumption	**Transceiver**	TX 29μW / RX 11.2μW
	Switch	2.7mW
	Compensator	0.17mW
Die Area	**Transceiver & Switch**	1.56 x 1.28mm^2
	Compensator	1.08 x 0.74mm^2

V. IMPLEMENTATION RESULTS

The proposed wearable network system and the RC are implemented in respectively, in 0.25-μm one-poly five-metal (1P5M) CMOS technology. The measured results of the wireless link before and after the compensation are shown in Fig. 15. It indicates that the RC reduces the effective inductance variation by 81%, from 1.51 μH to 0.31 μH, thereby reducing variances of received input pulse swing (V_{RECV}). As a result, V_{RECV} is increased by 14% in the measurement. Fig. 16 is the microphotograph of the transceiver with the switch, and the RC, which occupies 2.0 mm^2 and 0.8 mm^2, respectively, including pads.

The performance of the proposed system is summarized in Table IV. Fig. 17 and Table V summarize the performance comparison with previous works. The reception energy (energy per bit of the receiver) of the proposed transceiver is only 1.12 pJ/b at 10 Mbps, which is 75% and 21% of those of 90-nm and 0.18-μm chips, respectively, in [14] with clock link power included. The clock link power is included for fair comparison, since synchronous links such as [14] or [15] require clock transmission as well as data transmission to communicate between layers; in contrast, the proposed system adopts an asynchronous link without using any clock link. The clock link power of 90-nm chip is not reported in [14], so it is estimated by scaling down the reported clock link power of 0.18-μm chip.

A demonstration with a portable music player and an earset are shown in Fig. 18. MP3 music stream is transmitted via intra-layer wearable network, and the earset is connected to inter-layer link in shoulder. Music stream is successfully recovered and played in the earset.

VI. CONCLUSION

A low energy inductive-coupling transceiver with a fault-tolerant network switch is proposed and implemented to form an energy-efficient inter- and intra-layer wearable network. The proposed system is the first CMOS implantation to integrate both inter- and intra-layer wearable network at the same time. The proposed system considers the unique wearable network characteristics. The inductive coupling transceiver adopts resonance compensator with digitally controlled capacitor bank to compensate the time- and spatial varying woven inductor, and it enables low power wireless transaction with the reception energy of only 1.12 pJ/b at 2.5 V supply. The proposed

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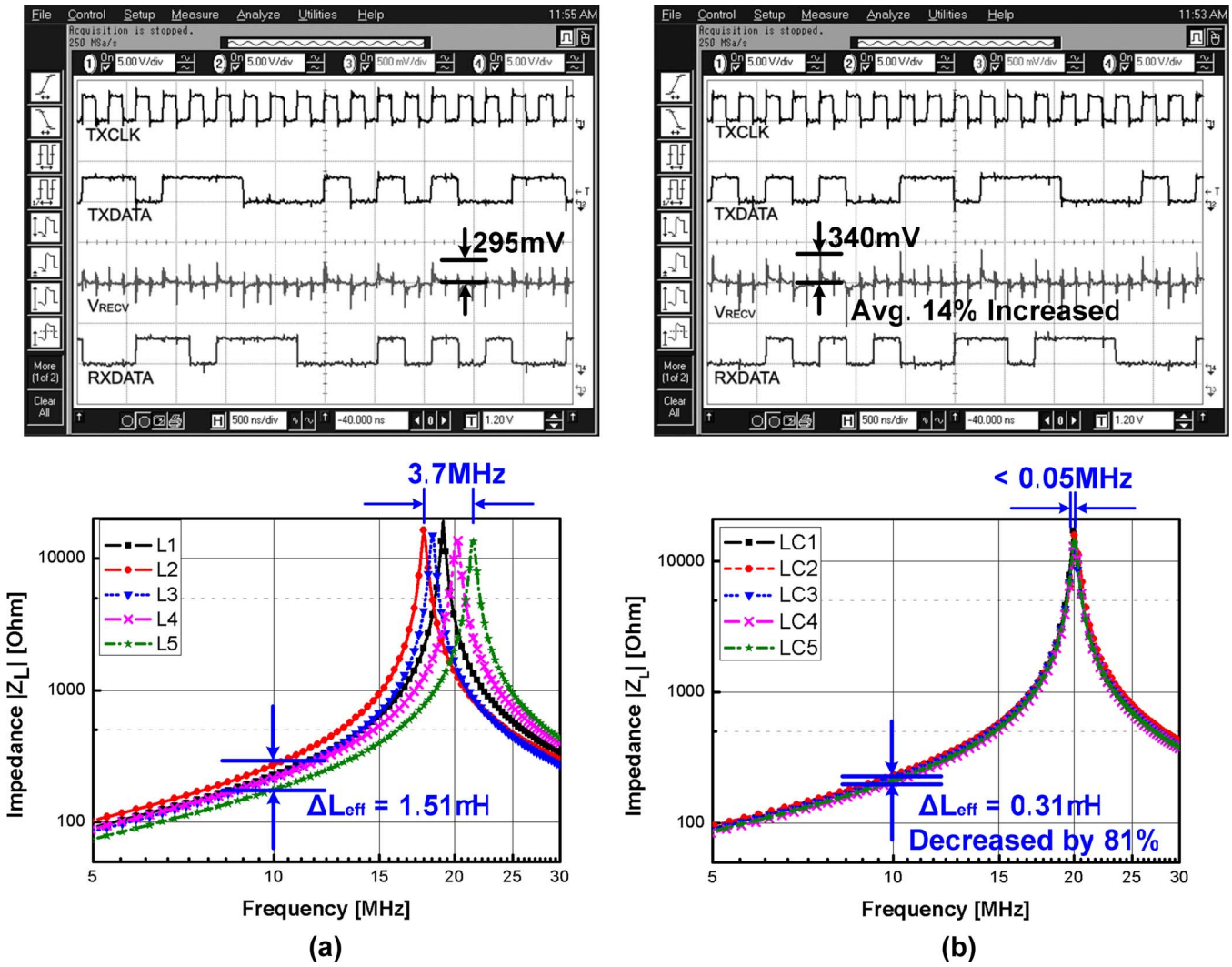

Fig. 15. Measurement results for the wireless link (a) before and (b) after the compensation.

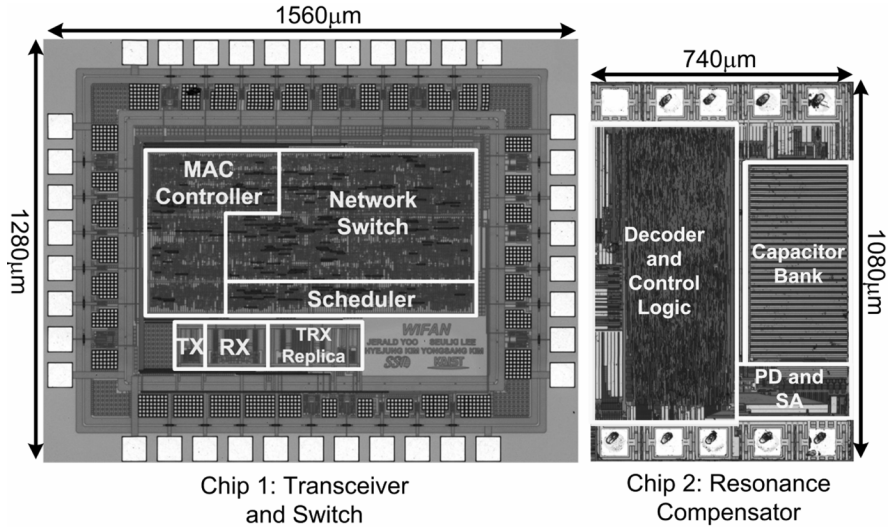

Fig. 16. Chip microphotographs.

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TABLE V
COMPARISON WITH PREVIOUS WORKS

Parameters	[7]	[8]	[9]	[15]	This Work
Energy / bit	-	-	0.62nJ/b	56nJ/b	1.12pJ/b
Antenna Size (Diameter)	-	Bulky (>15cm)	-	Small	Small (<2cm)
Wireless Interface	RFID	RFID	Bluetooth	Inductive	Inductive
Data Rate	-	125kbps	256kbps	100kbps	10Mbps
Chip Implementation	X	X	X	X	O
Inter-Layer Communication	X	O	X	O	O
Fault Tolerance	O	X	O	X	O

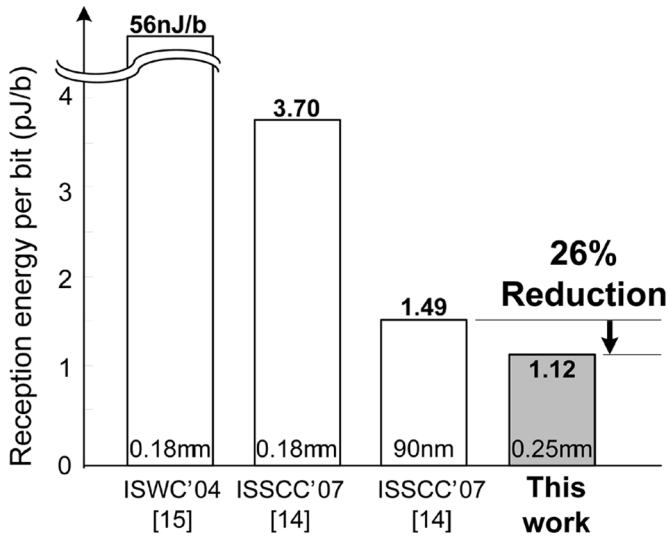

Fig. 17. Reception energy comparison with previous works.

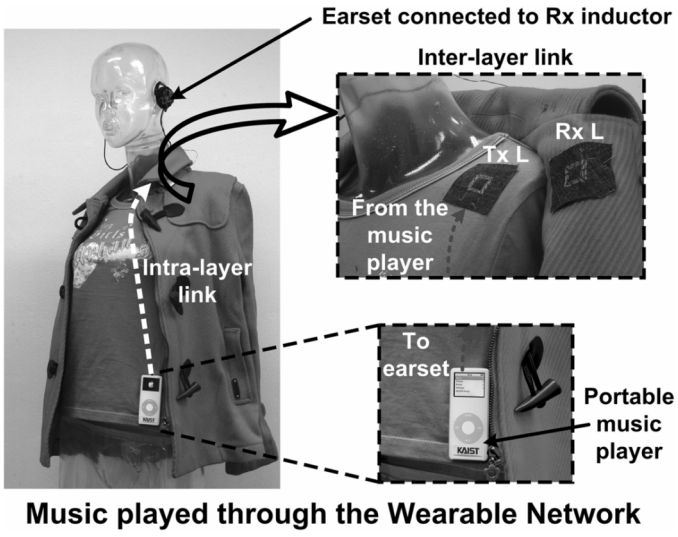

Fig. 18. Wearable network portable music player demonstration.

network switch introduces new fault-tolerant protocol to provide fault-tolerance, and the switch eliminates the routing table to reduce power consumption by 70% compared with the conventional switch using torus topology. The proposed transceiver with the network switch and the RC occupies 2.0 mm^2 and 0.8 mm^2, respectively, in 0.25-μm 1P5M CMOS technology.

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