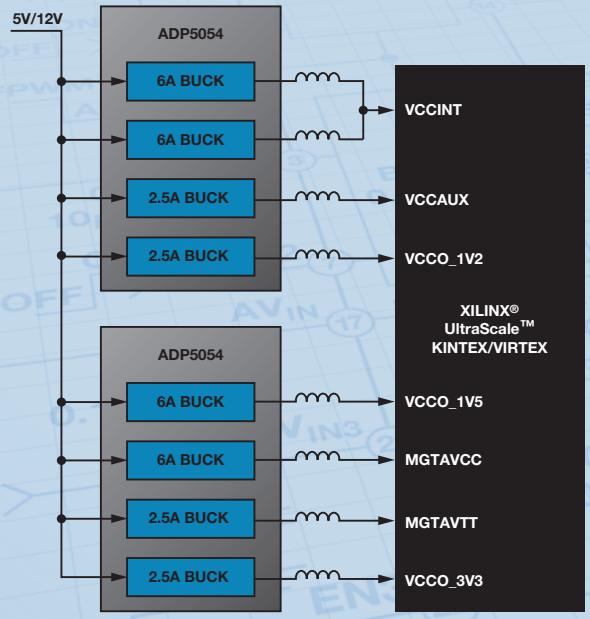
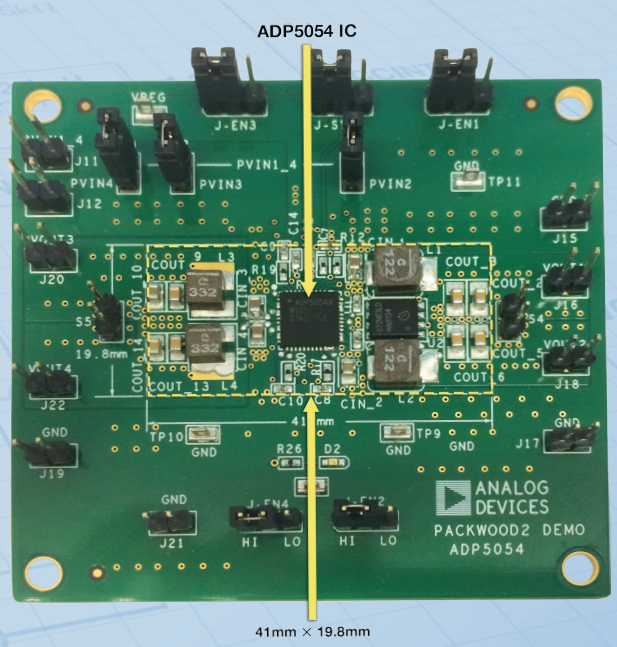
Integrated, High Power Solutions for Xilinx FPGAs

Modern, high performance, FPGA-based systems require an increasing number of dedicated rails supplying core, I/O, memory, PLL, and precision analog voltages. Typical FPGA-based systems today make use of standalone switching regulators and LDOs, but as board area continues to shrink as end product form factors shrink, this complicates the task of designing more efficient power management solutions for powering FPGAs. Combining multiple switching regulators and LDOs into a single package enables very small, flexible, highly efficient power management solutions for powering FPGAs and precision analog components with the highest system reliability.

Ultrasmall 12 V/5 V Quad Buck in LFCSP



ADP5054 Solution Size Only 41 mm × 20 mm



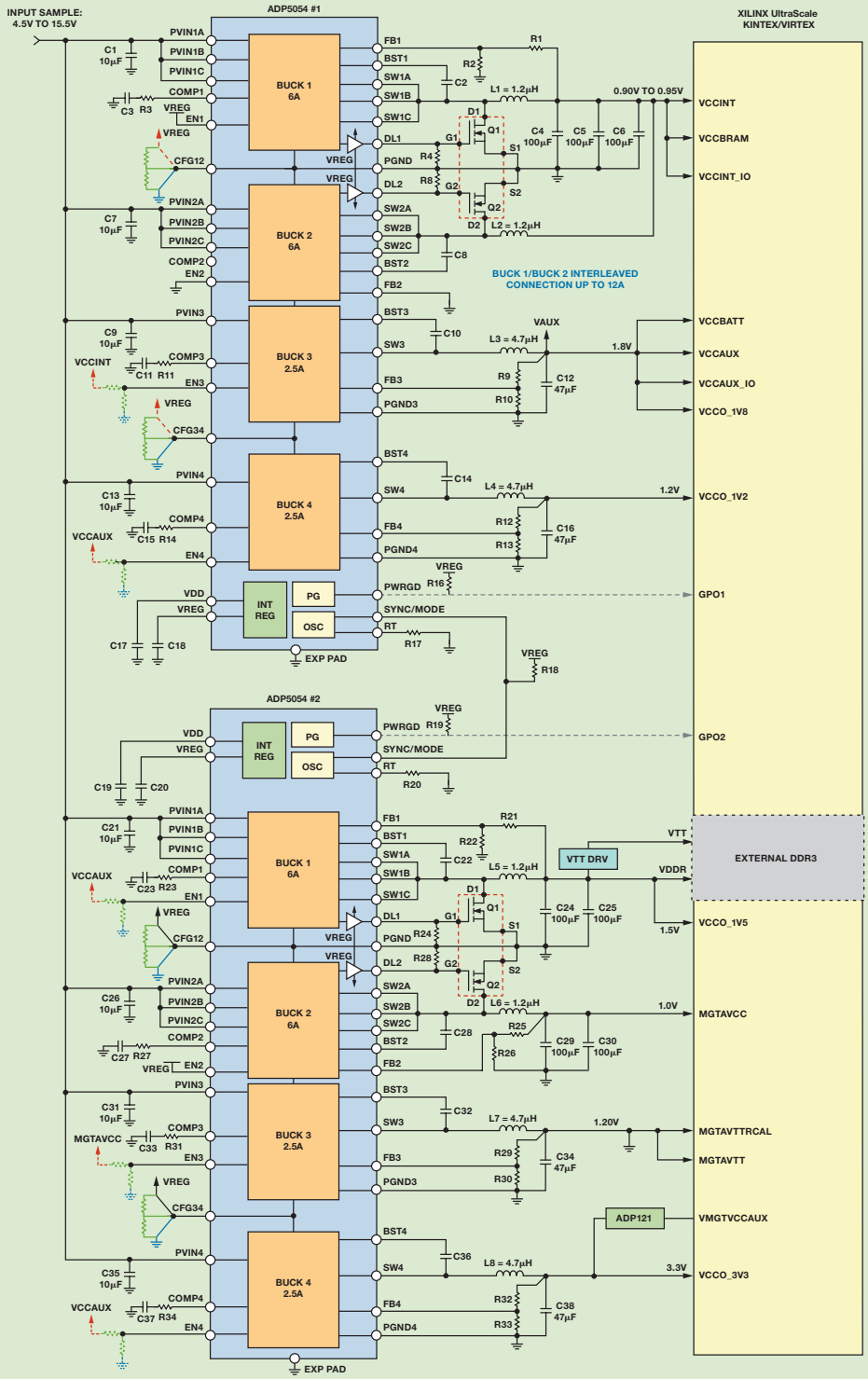
- *Fixed and Adjustable Output Voltages*
- *Wide Range of Switching Frequency Operation (250 kHz to 2 MHz)*
- *Resistor Programmable Current Limit on Buck 1 and Buck 2 (6 A, 4 A, 2 A)*
- *Simple Power Supply Sequencing*
- *Frequency Synchronization Input or Output*
- *Parallel Operation on Buck 1 and Buck 2, and Buck 3 and Buck 4*

XILINX®

analog.com/multioutput-regulators

ANALOG DEVICES

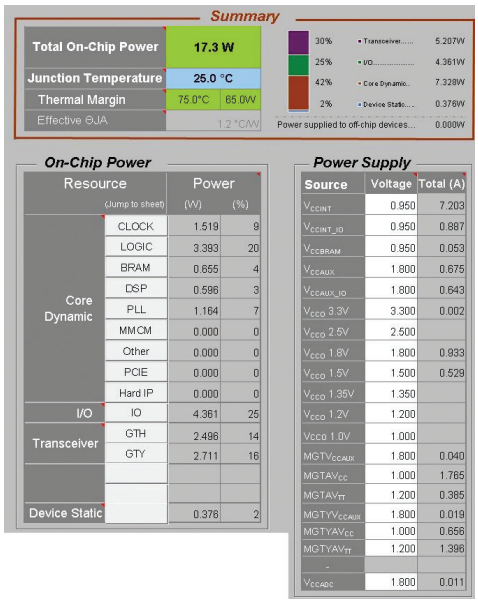
ADP5054 Supply for Xilinx UltraScale Kintex/Virtex



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1]Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2]Resistor programmable current limit (6 A, 4 A, or 2 A).

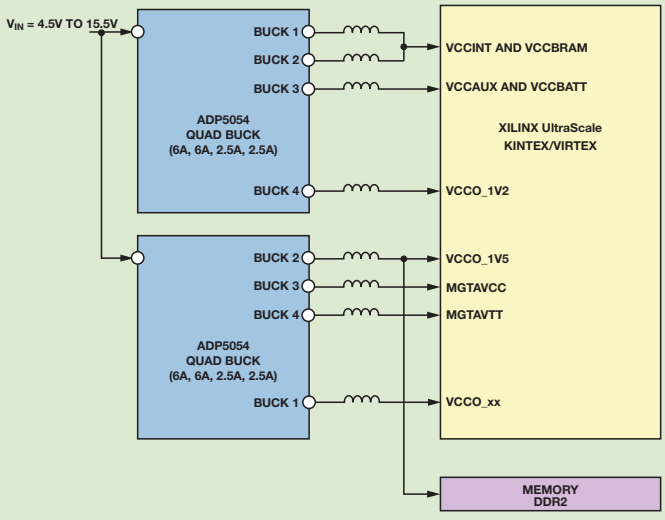
Xilinx Power Estimator (XPE)—Use Cases for Xilinx UltraScale Kintex/Virtex



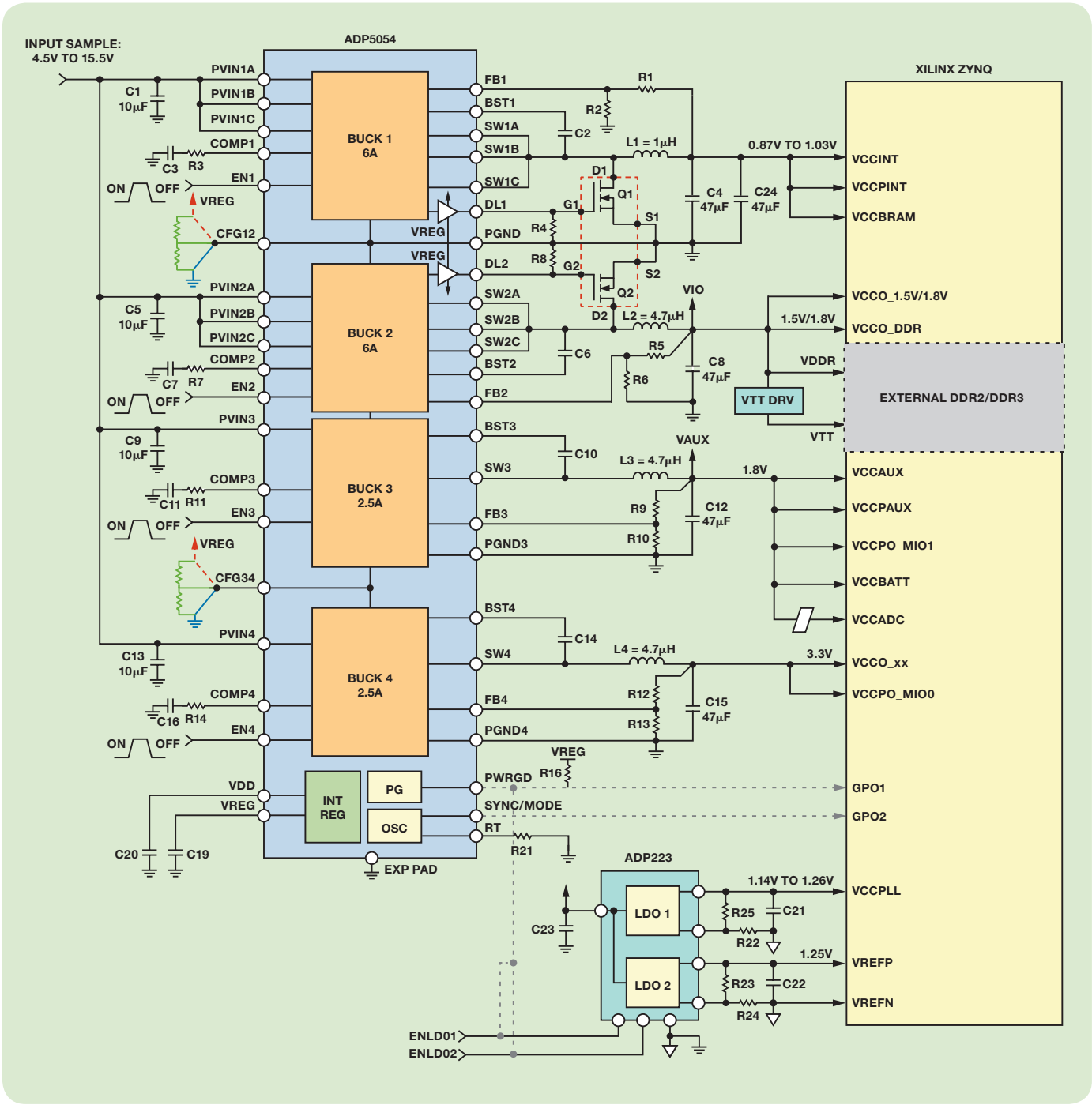
Bill of Materials for the ADP5054 Powering Xilinx UltraScale Kintex/Virtex

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1, U2	2	4-channel micro PMU	ADP5054ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C8, C10, C14, C22, C28, C32, C36	8	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C7, C9, C13, C21, C26, C31, C35	8	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C5, C6, C24, C25	5	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C16, C29, C30, C34, C38	6	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C3, C11, C15,C23, C27, C33, C37	7	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1(Q2), Q3(Q4)	2	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1, L2, L5, L6	4	1.2 µH, 22 A, 6.8 mΩ	XAL6030-122ME	Coilcraft	6.0 × 6.0 × 3.0	
		1.3 µH, 8.2 A, 16 mΩ	NRS6045-1R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L3, L4, L7, L8	4	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R17, R20	2	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8, R24, R28	4	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R3, R9, R10, R11, R12, R13, R14, R21, R22, R23, R25, R26, R27, R29, R30, R31, R32, R33, R34	21	Resistor, 1%		Various	0402	Values depend on output voltage setting
R16, R18	2	10 kΩ, resistor, 5%		Various	0402	

Simplified Application Diagram for the ADP5054 Powering Xilinx UltraScale Kintex/Virtex



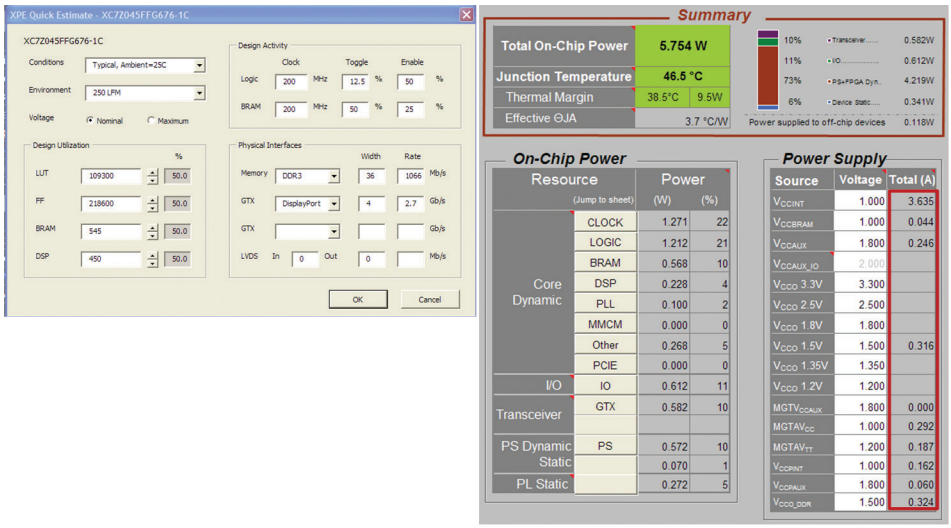
ADP5050 Supply for Xilinx Zynq



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2] Resistor programmable current limit (6 A, 4 A, or 2 A).

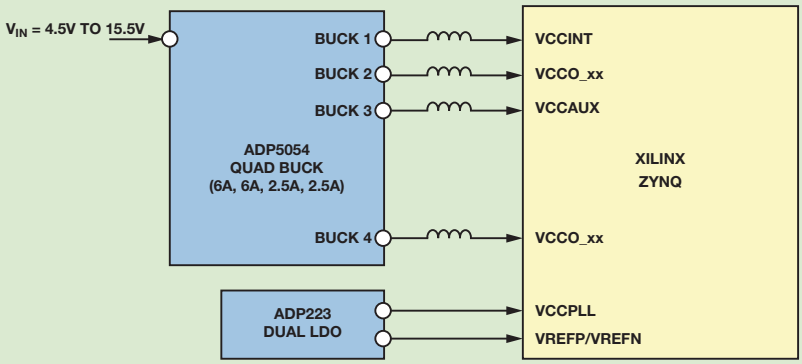
XPE Power Estimation—Use Cases for Xilinx Zynq



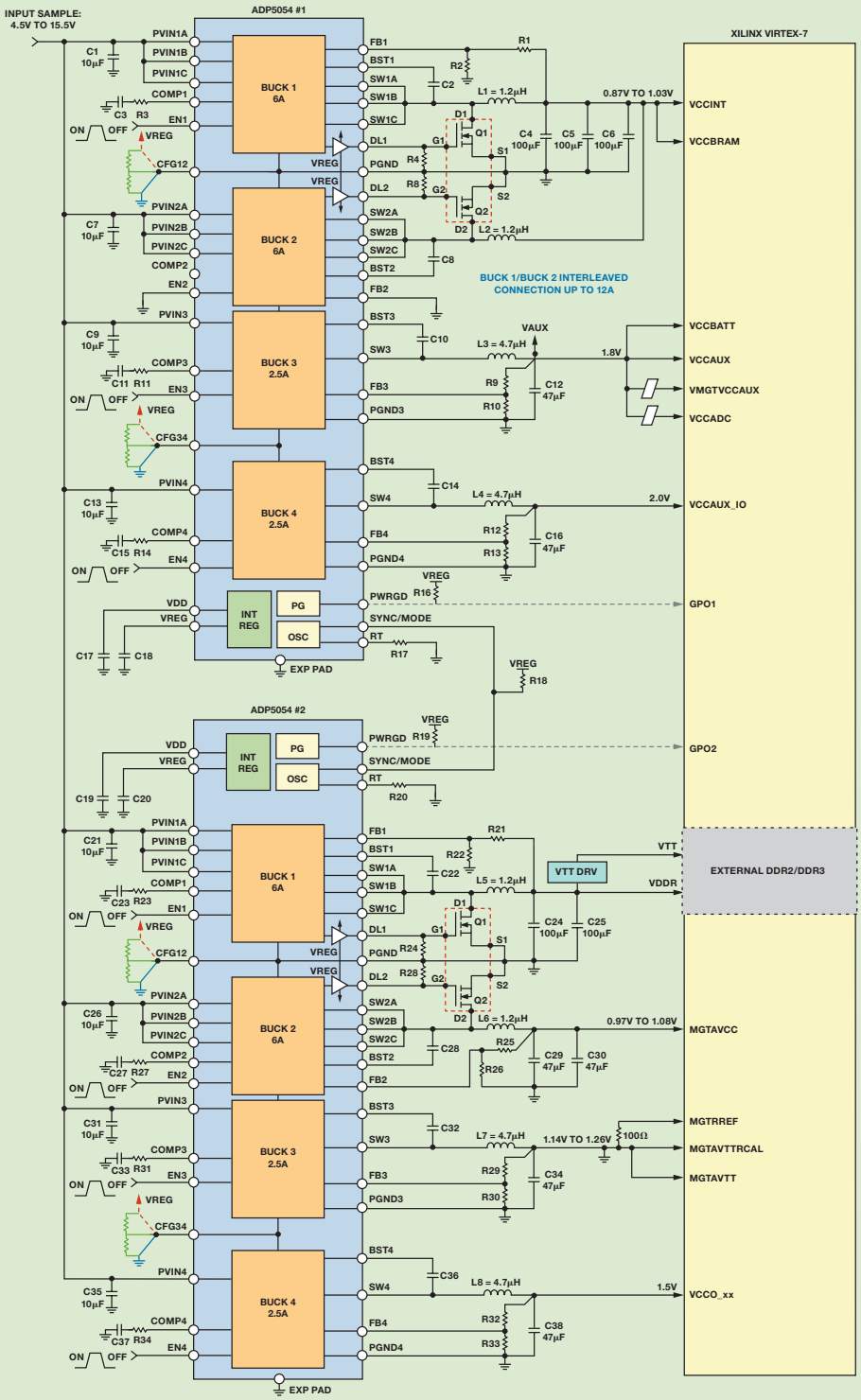
Bill of Materials for the ADP5054 Powering Xilinx Zynq

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	4-channel micro PMU	ADP5054ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
U2	1	Dual 300 mA LDO	ADP223ACPZ	ADI	2.0 × 2.0 × 0.55 QFN	
C17, C18, C21, C22, C23	5	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C8, C24	3	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C15	2	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C3, C7, C11, C16	4	2.2 nF, X5R, 25V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 5 A, 54 mΩ	FDMA1024NZ	Fairchild	2.0 × 2.0 × 0.8 QFN	
		Dual N-FETs, 20 V, 4.5 A, 46 mΩ	SIA906EDJ	Vishay	2.0 × 2.0 × 0.8 QFN	
L1	1	1.2 µH, 22 A, 6.8 mΩ	XAL6030-122ME	Coilcraft	6.0 × 6.0 × 3.0	
		1.3 µH, 8.2 A, 16 mΩ	NRS6045-1R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L2, L3, L4	3	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R17	1	38.4 kΩ, resistor, 1%		Various	0402	
R4	1	22 kΩ, resistor, 5%		Various	0402	
R8	1	47 kΩ, resistor, 5%		Various	0402	
R1, R2, R3, R5, R6, R7, R9, R10, R11, R12, R13, R14, R22, R23, R24, R25	16	Resistor, 1%		Various	0402	Values depend on output voltage setting
R16	1	10 kΩ, resistor, 5%		Various	0402	

Simplified Application Diagram for the ADP5054 Powering Xilinx Zynq



ADP5054 Supply for Xilinx Virtex-7



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1]Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2]Resistor programmable current limit (6 A, 4 A, or 2 A).

XPE Power Estimation—Use Cases for Xilinx Virtex-7

Xilinx FPGA Selection		Power Estimation Conditions—Xilinx XPower v14.3[1]													
Family	Logic Elements	Clock Low Speed (MHz)	Low Speed Logic Used (%)	Toggle Rate (%)	Clock High Speed (MHz)	High Speed Logic Used (%)	Toggle Rate (%)	DSP/ Slices	BRAM Blocks	RAM Clock (MHz)	Outputs	I/O Toggle Rate (MHz)	Out Load (pF)	XCVR Frequency	XCVR Channels (GHz)
Virtex-7	≤978 k	100	40	25.00	600	10.00	12.50	1000 @ 400 MHz	1500	400	200	100	10	8	10

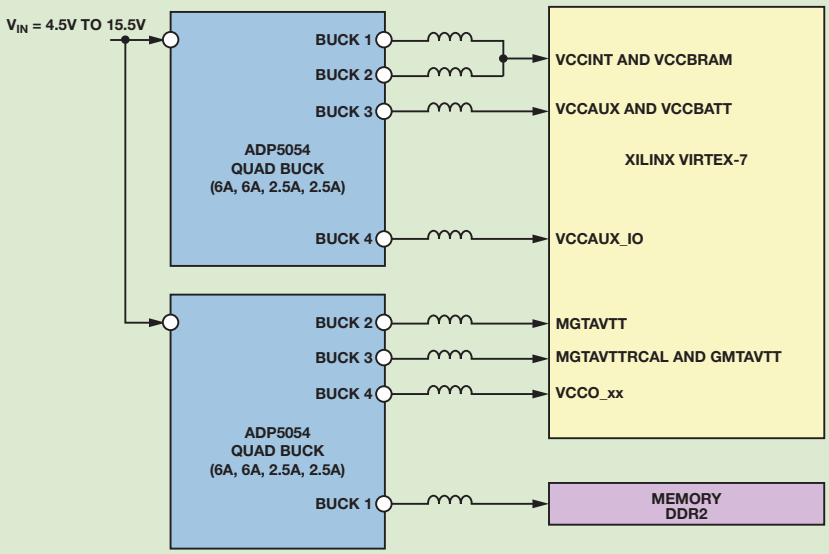
FPGA Power Consumption Derived from Spreadsheet				
ICCINT[2]	ICCIO_1V5 (DDR3 Support)	ICCAUX, ICCO_1V8	IMGT_AVCC[3]	IMGT_AVTT
7.65 A (@ 1.0 V)	0.1 A (@ 1.5 V)	0.32 A (@ 1.8 V)	1 A (@ 1.05 V)	0.36 A (@ 1.2 V)

[1] Power requirement derived from Xilinx XPE 14.3—the spreadsheet assumes at least 50% of resources occupation.
[2] 4 A to 8 A core current requirement can be achieved by connecting the ADP505x Buck 1 and Buck 2 in interleaved configuration (see Virtex-7 application diagram).
[3] Assumes 1.8 V I/O domain and DDR3 control interface, assumes external DDR3 VTT termination driver.

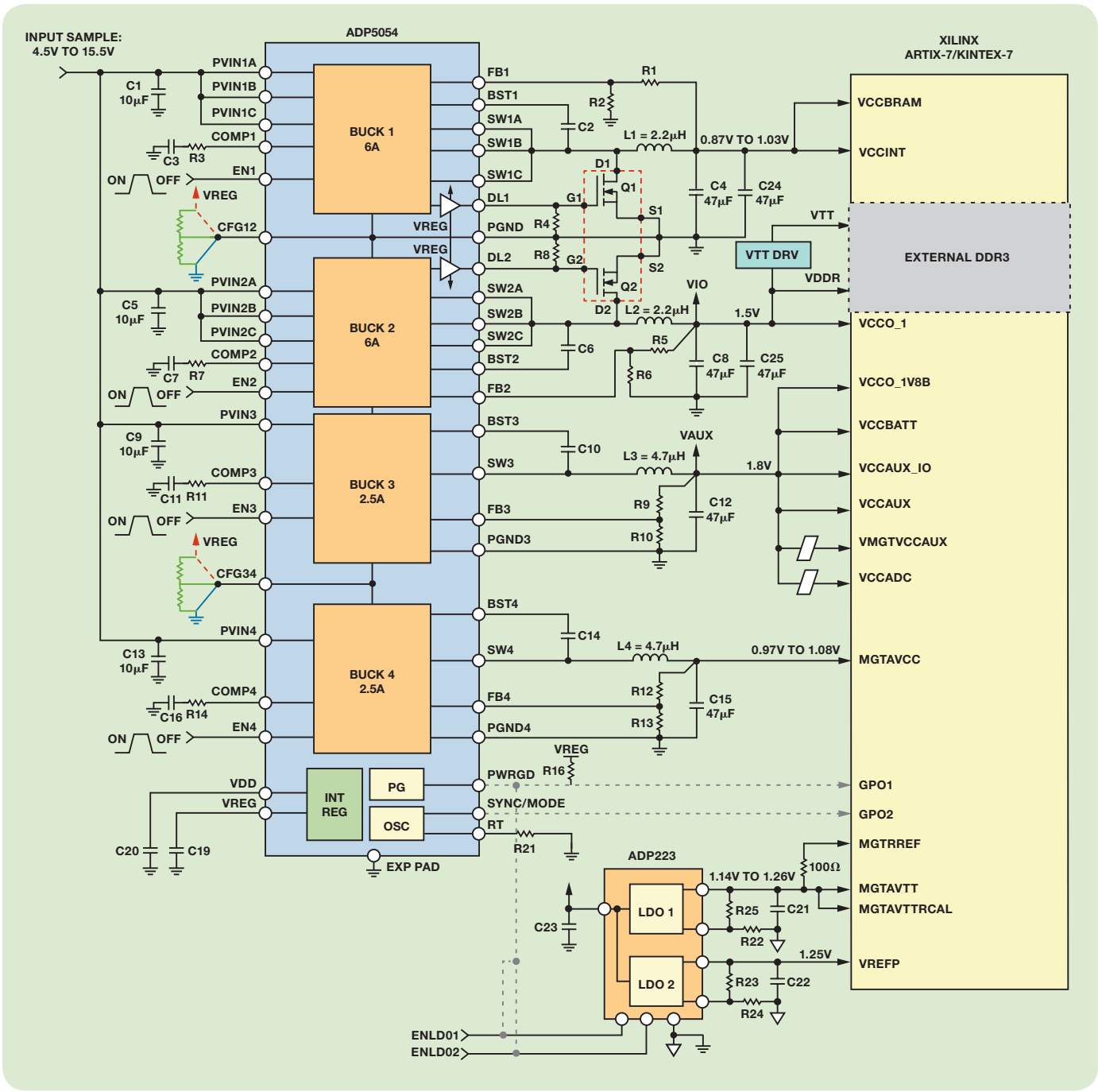
Bill of Materials for the ADP5054 Powering Xilinx Virtex-7

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1, U2	2	4-channel micro PMU	ADP5054ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
C17, C18, C19, C20	4	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C8, C10, C14, C22, C28, C32, C36	8	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C7, C9, C13, C21, C26, C31, C35	8	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C5, C6, C24, C25	5	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C16, C29, C30, C34, C38	6	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C3, C11, C15,C23, C27, C33, C37	7	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1(Q2), Q3(Q4)	2	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 23 A, 25 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1, L2, L5, L6	4	2.2 µH, 15.9 A, 12.7 mΩ	XAL6030-222ME	Coilcraft	6.0 × 6.0 × 3.0	
		2.3 µH, 6.4 A, 22 mΩ	NRS6045-2R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L3, L4, L7, L8	4	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R17, R20	2	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8, R24, R28	4	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R3, R9, R10, R11, R12, R13, R14, R21, R22, R23, R25, R26, R27, R29, R30, R31, R32, R33, R34	21	Resistor, 1%		Various	0402	Values depend on output voltage setting
R16, R18	2	10 kΩ, resistor, 5%		Various	0402	

Simplified Application Diagram for the ADP5054 Powering Xilinx Virtex-7



ADP5054 Supply for Xilinx Artix-7/Kintex-7



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1]Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2]Resistor programmable current limit (6 A, 4 A, or 2 A).

XPE Power Estimation—Use Cases for Xilinx Artix-7/Kintex-7

Xilinx FPGA Selection		Power Estimation Conditions—Xilinx XPower v14.3[1]													
Family	Logic Elements	Clock Low Speed (MHz)	Low Speed Logic Used (%)	Toggle Rate (%)	Clock High Speed (MHz)	High Speed Logic Used (%)	Toggle Rate (%)	DSP/ Slices	BRAM Blocks	RAM Clock (MHz)	Outputs	I/O Toggle Rate (MHz)	Out Load (pF)	XCVR Frequency	XCVR Channels (GHz)
Kintex-7	≤326 k	100	40	25.00	600	15.00	12.50	500 @ 400 MHz	500	400	200	100	10	4	3
Kintex-7	≤478 k	100	35	25.00	600	10.00	12.50	1000 @ 400 MHz	1000	400	200	100	10	4	5
Virtex-7	≤978 k	100	40	25.00	600	10.00	12.50	1000 @ 400 MHz	1500	400	200	100	10	8	10

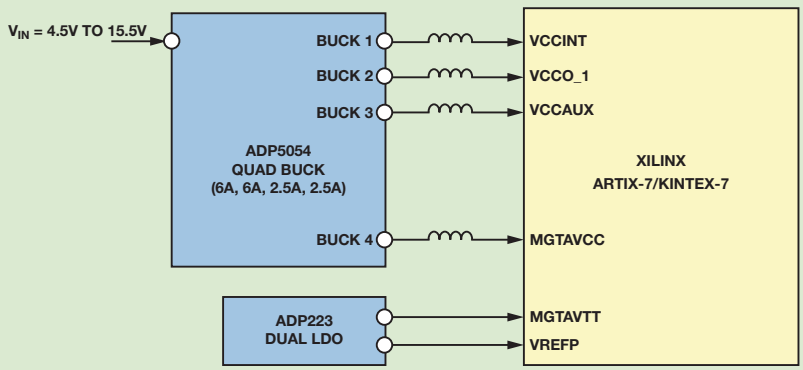
FPGA Power Consumption Derived from Spreadsheet				
ICCINT[2]	ICCIO_1V5 (DDR3 Support)	ICCAUX, ICCO_1V8[3]	IMGT_AVCC	IMGT_AVTT
3.15 A (@ 1.2 V)	0.1 A (@ 1.5 V)	0.32 A (@ 1.8 V)	0.511 A (@ 1.0 V)	0.36 A (@ 1.2 V)
4.23 A (@ 1.0 V)	0.1 A (@ 1.5 V)	0.32 A (@ 1.8 V)	0.57 A (@ 1.0 V)	0.31 A (@ 1.2 V)
7.65 A (@ 1.0 V)	0.1 A (@ 1.5 V)	0.32 A (@ 1.8 V)	1 A (@ 1.05 V)	0.36 A (@ 1.2 V)

[1] Power requirement derived from Xilinx XPE 14.3—the spreadsheet assumes at least 50% of resources occupation.
[2] 4 A to 8 A core current requirement can be achieved by connecting the ADP505x Buck 1 and Buck 2 in interleaved configuration (see Artix-7/Kintex-7 application diagram).
[3] Assumes 1.8 V I/O domain and DDR3 control interface, assumes external DDR3 VTT termination driver.

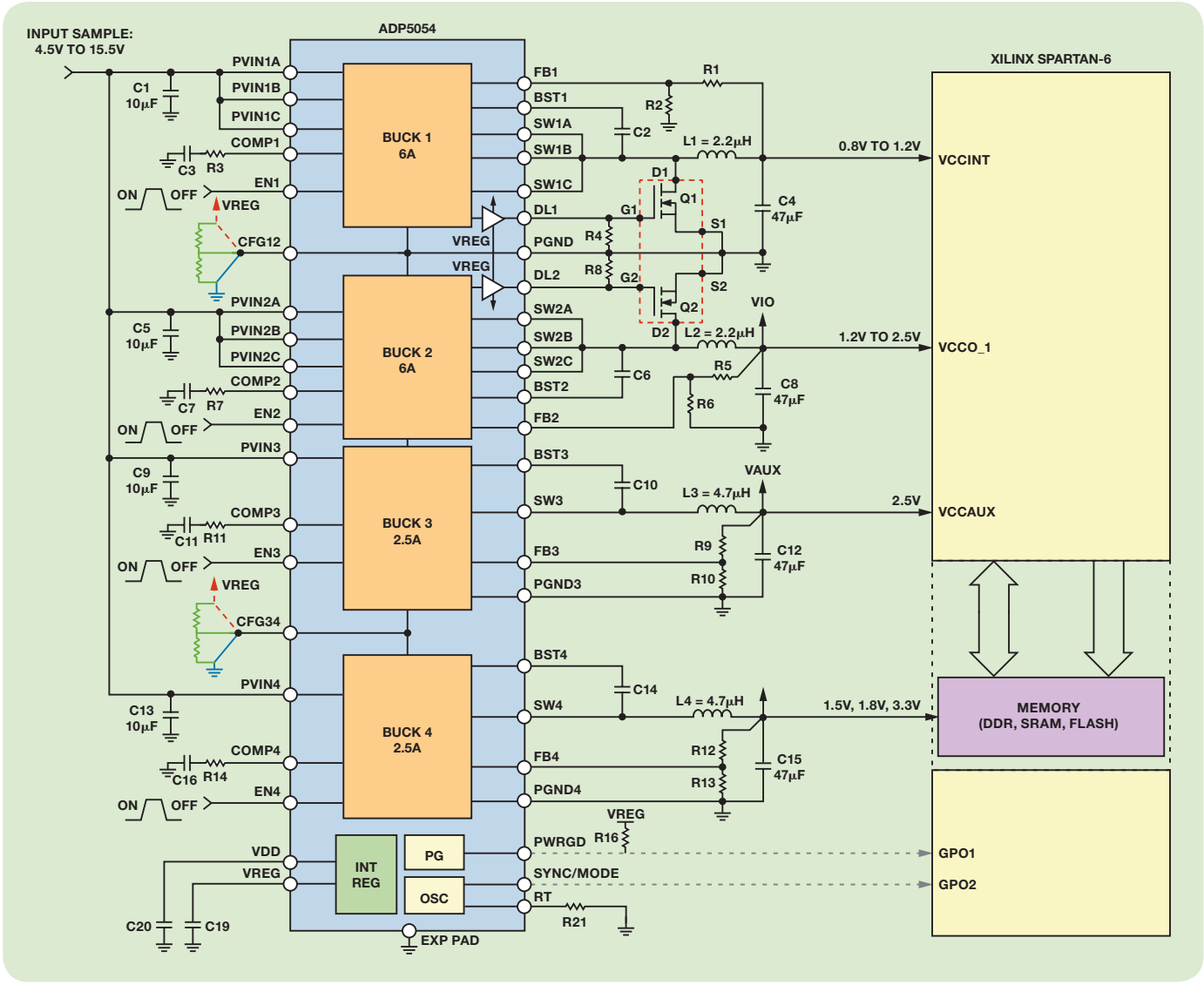
Bill of Materials for the ADP5054 Powering Xilinx Artix-7/Kintex-7

Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	4-channel micro PMU	ADP5054ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
U2	1	Dual 300 mA LDO	ADP223ACPZ	ADI	2.0 × 2.0 × 0.55 QFN	
C17, C18, C21, C22, C23	5	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C8, C24, C25	4	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C15	2	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C3, C7, C11, C16	4	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 25 A, 16 mΩ	Si7232DN	Vishay	3.3 × 3.3 × 1.0 QFN	
		Dual N-FETs, 30 V, 10 A, 20 mΩ	IRFHM8364	IR	3.3 × 3.3 × 0.9 QFN	
L1, L2	2	2.2 µH, 15.9 A, 12.7 mΩ	XAL6030-222ME	Coilcraft	6.0 × 6.0 × 3.0	
		2.3 µH, 6.4 A, 22 mΩ	NRS6045-2R3NMGK	Taiyo Yuden	6.0 × 6.0 × 4.5	
L3, L4	2	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R17	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	22 kΩ, resistor, 5%		Various	0402	
R1, R2, R3, R5, R6, R7, R9, R10, R11, R12, R13, R14, R22, R23, R24, R25	16	Resistor, 1%		Various	0402	Values depend on output voltage setting
R16	1	10 kΩ, resistor, 5%		Various	0402	

Simplified Application Diagram for the ADP5054 Powering Xilinx Artix-7/Kintex-7



ADP5054 Supply for Xilinx Spartan-6



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1]Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2]Resistor programmable current limit (6 A, 4 A, or 2 A).

XPE Power Estimation—Usage Case for Spartan-6

Xilinx FPGA Selection		Power Estimation[1]													
Family	Logic Elements	Clock Low Speed (MHz)	Low Speed Logic Used (%)	Toggle Rate (%)	Clock High Speed (MHz)	High Speed Logic Used (%)	Toggle Rate (%)	DSP/ Instances	RAM Blocks	RAM Clock (MHz)	Outputs	I/O Toggle Rate (MHz)	Out Load (pF)	XCVR Frequency	XCVR Channels
Spartan-6	<150 k	100	40	12.50	600	15.00	12.50	36 × 36 mult/80	150	100	150	50	30	N/A	N/A
Spartan-6 with XCVR	<150 k	100	40	12.50	600	15.00	12.50	36 × 36 mult/80	150	300	150	50	30	4	1.25 GHz

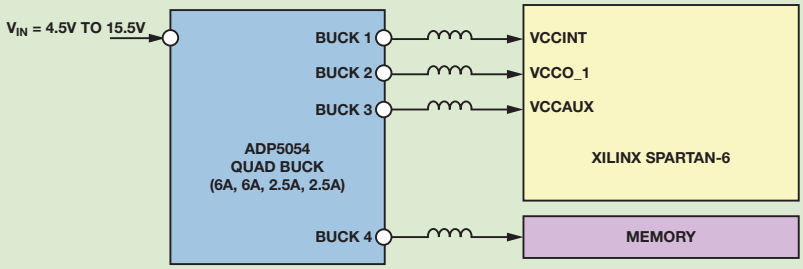
FPGA Power Consumption Derived from Spreadsheet[2]				
ICCINT + ICC	ICCIO + ICCPO + ICCPO	ICCAUX	MGT_VCC_PLL	MGT_Tx_Rx
1.658 A (@ 1.2 V)	0.039 A (@ 2.5 V)	0.051 A (@ 2.5 V)	N/A	N/A
1.82 A (@ 1.2 V)	0.039 A (@ 2.5 V)	0.066 A (@ 2.5 V)	0.29 A (@ 1.2 V)	0.18 A (@ 1.2 V)

[1] Power requirement derived from Xilinx XPE 13.3—the spreadsheet assumes at least 50% of resources occupation with 12.5% toggle rate. The core current is kept below the maximum driving capability of the suggested micro PMU.
[2] The proposed micro PMU supplies three FPGA rails: VCCINT, VCCO, and VCCAUX from Buck 1, Buck 2, and Buck 3, respectively. Buck 2 and Buck 3 have spare power to power external peripheral devices and static or low power DDR memories. Only one I/O supply voltage is considered, and multiple I/O banks with different voltage levels can be supported.

Bill of Materials for the ADP5054 Powering Xilinx Spartan-6

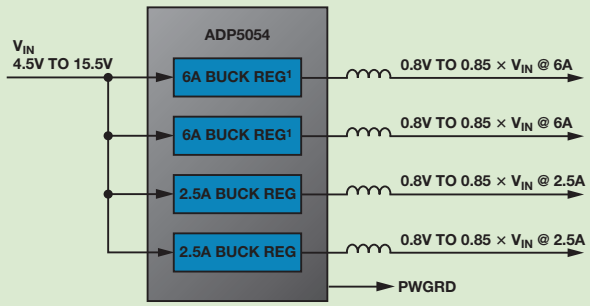
Reference	Quantity	Value	Part Number	Vendor	Footprint (mm)	Notes
U1	1	4-channel micro PMU	ADP5054ACPZ	ADI	7.0 × 7.0 × 0.75 QFN	
C17, C18	2	1 µF, X5R, 6.3 V	GRM155R60J105KE19D	Murata	0402	
C2, C6, C10, C14	4	0.1 µF, X5R, 16 V	GRM155R61C104KA88D	Murata	0402	
C1, C5, C9, C13	4	10 µF, X5R, 25 V	GRM219R61E106KA12	Murata	0805	
C4, C8	2	100 µF, X5R, 6.3 V	GRM31CR60J107ME39	Murata	1206	
C12, C15	2	47 µF, X5R, 6.3 V	GRM21BR60J476ME15	Murata	0805	
C3, C11, C16	3	2.2 nF, X5R, 25 V	GRM155R61E222KA01D	Murata	0402	
Q1 (Q2)	1	Dual N-FETs, 20 V, 5 A, 54 mΩ	FDMA1024NZ	Fairchild	2.0 × 2.0 × 0.8 QFN	
		Dual N-FETs, 20 V, 3.4 A, 45 mΩ	IRLHS6276	IR	2.0 × 2.0 × 0.8 QFN	
		Dual N-FETs, 20 V, 4.5 A, 46 mΩ	SIA906EDJ	Vishay	2.0 × 2.0 × 0.8 QFN	
L1, L2	2	2.2 µH, 3.7 A, 21 mΩ	XFL4020-222ME	Coilcraft	4.0 × 4.0 × 2.0	
		2.2 µH, 3.0 A, 42 mΩ	NRS4018T-2R2MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
L3, L4	2	4.7 µH, 2.7 A, 57 mΩ	XFL4020-472ME	Coilcraft	4.0 × 4.0 × 2.0	
		4.7 µH, 2.0 A, 70 mΩ	NRS4018T-4R7MDGJ	Taiyo Yuden	4.0 × 4.0 × 1.8	
R17	1	38.4 kΩ, resistor, 1%		Various	0402	
R4, R8	2	No assembly		Various	0402	
R1, R2, R3, R9, R10, R11, R12, R13, R14	9	Resistor, 1%		Various	0402	Values depend on output voltage setting
R16	1	10 kΩ, resistor, 5%		Various	0402	

Simplified Application Diagram for the ADP5054 Powering Xilinx Spartan-6

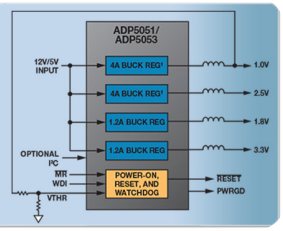


ADP5054 and ADP5050/ADP5051/ADP5052/ADP5053

ADP5054 Quad Buck Switching Regulator in LFCSP



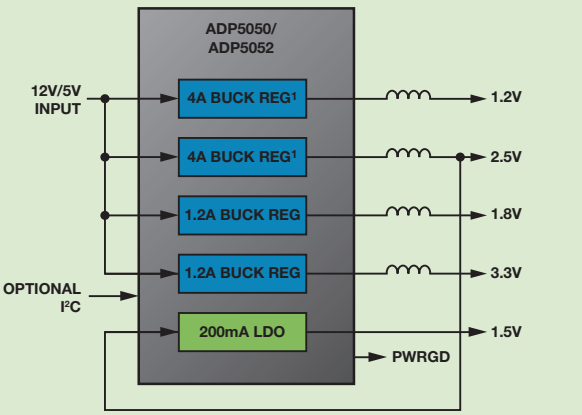
[1] Resistor programmable current limit (6 A, 4 A, or 2 A).

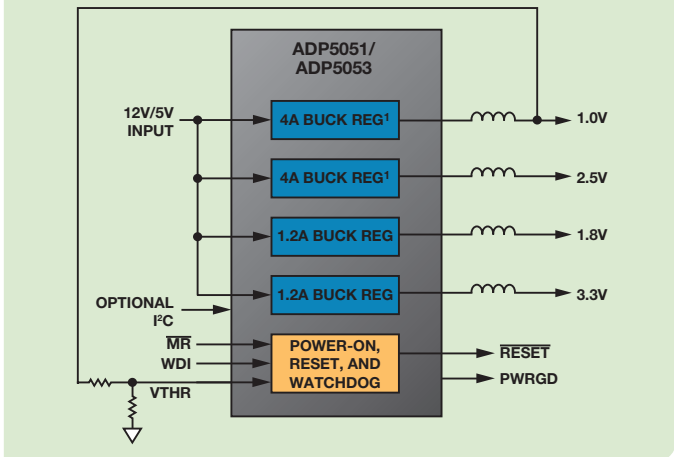


Key Features

- CH1/CH2: programmable 2 A/4 A/6 A sync buck regulator with low-side FET driver
  - Parallel CH1/CH2 to deliver up to 12 A output
- CH3/CH4: 2.5 A buck regulator
  - Parallel CH3/CH4 to deliver up to 5 A output
- Wide input range: 4.5 V to 15.5 V
- Resistor adjustable or fixed output voltage
- 250 kHz ~ 2 MHz adjustable switching frequency
- ½ × f_{SW} selective for each channel
- Precision enable on accurate 0.8 V threshold
- Programmable current limit in CH1/CH2
- Soft start timer programmable
- FPWM/PSM mode selection
- Active output discharge switch
- PWRGD flag on selective channels
- Frequency synchronization input or output
- Hiccup or latch-off for output short protection
- UVLO, OCP, TSD
- 7 mm × 7 mm, 48-lead LFCSP package

ADP5050/ADP5051/ADP5052/ADP5053 Quad Buck Switching Regulator with LDO or POR/WDI in LFCSP





[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

Key Features

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory
- Pseudo DVS (dynamic voltage scaling)
- I²C interface with interrupt supportive on fault condition
- CH1/CH2: programmable 1.2 A/2.5 A/4 A sync buck regulator with low-side FET driver
- CH3/CH4: 1.2 A sync buck regulator
- CH5: 200 mA low dropout LDO or watchdog timer and power-on reset
- Precision enable on 0.8 V accurate threshold
- Active output discharge switch
- FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag on selective channels
- Startup with the precharged output
- 7 mm × 7 mm, 48-lead LFCSP package
- −40°C to +125°C junction temperature
- I²C functionality

Low Power, Spartan-6 Integrated Power Solutions

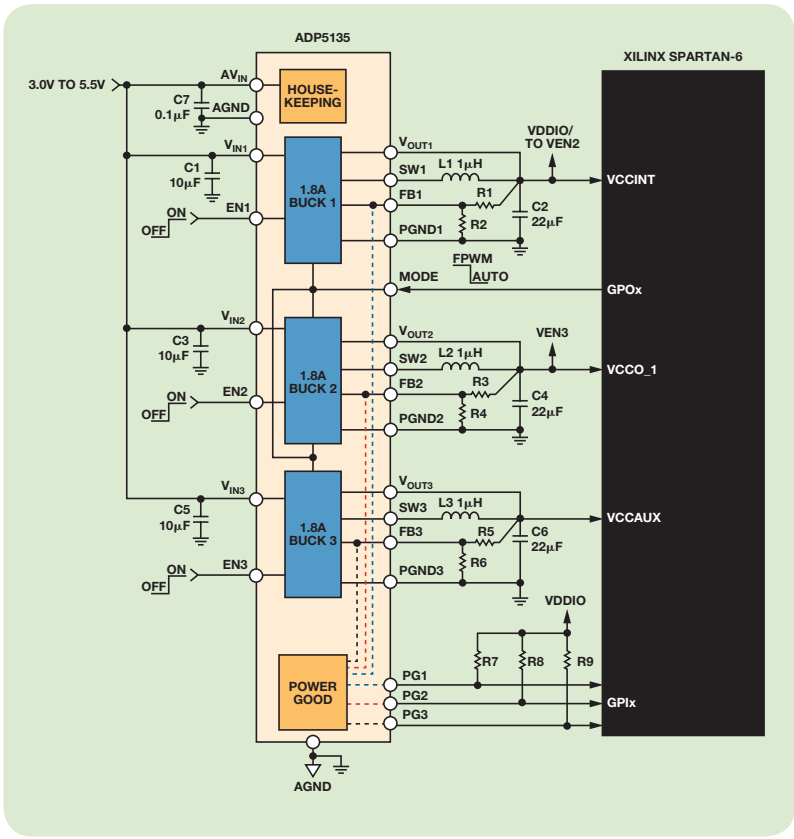
ADP5135: Triple, 1.8 A, 3 MHz Buck Regulator in LFCSP

Key Features

- Main input voltage range 3.0 V to 5.5 V
- Three 1800 mA buck regulators
- 4 mm × 4 mm, 24-lead LFCSP package
- Regulator accuracy of ±1.8%
- Individual, dedicated buck, power-good pins
- Precision enable pins for easier power sequencing
- 3 MHz buck operation with forced PWM and automatic PWM/PSM modes
- Buck output voltage range from 0.8 V to 3.8 V

Applications

- Power for processors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and radio frequency (RF) chipsets



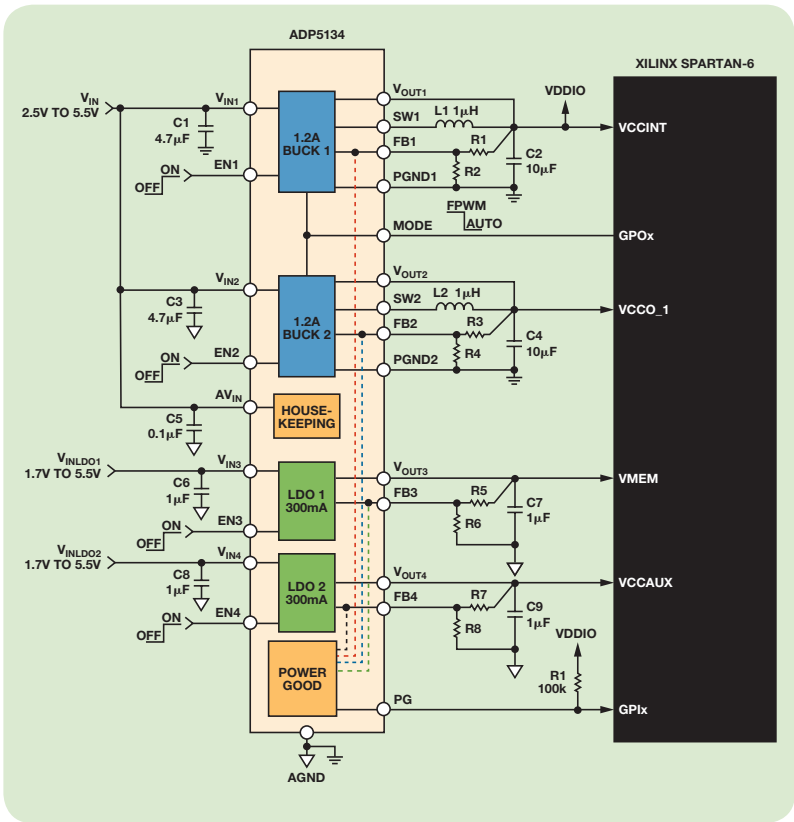
ADP5134: Dual, 3 MHz, 1.2 A Buck Regulator with Two 300 mA LDOs with Precision Enable and a Power Good in LFCSP

Key Features

- Main input voltage range 2.5 V to 5.5 V
- Two 1200 mA buck regulators and two 300 mA LDO regulators
- 4 mm × 4 mm, 24-lead LFCSP package
- Regulator accuracy of ±1.8%
- Factory programmable or external adjustable VOUTx
- Precision enable pin for easier power sequencing
- Factory selectable power-good pin
- 3 MHz buck operation with forced PWM and automatic PWM/PSM modes
- Buck 1/Buck 2: output voltage range from 0.8 V to 3.8 V
- LDO 1/LDO 2: output voltage range of 0.8 V to 5.2 V
- LDO 1/LDO 2: input voltage range from 1.7 V to 5.5 V
- LDO 1/LDO 2: high PSRR and low output noise

Applications

- Power for processors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and radio frequency (RF) chipsets



Integrated Power Management Solutions (Micro PMUs)

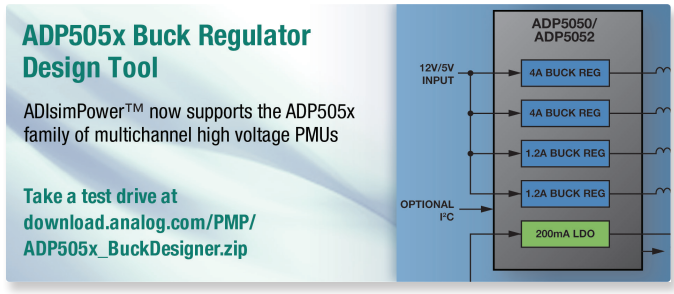
Part Number	Product Description	V_{IN} (V)	V_{OUT} (V)	Number of Outputs	Output Current (mA)	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Key Features	Package	Price 1k List ($U.S.)
ADP5022	Dual, 3 MHz buck with 150 mA LDO	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8	2 × buck	600	—	—	—	—	Mode pin, individual enable pins	16-ball WLCSP	1.80
		LDO: 1.7 to 5.5	LDO: 3.3, 3.0, 2.9, 2.8, 2.775, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	1 × LDO	150							
ADP5023	Dual, 800 mA buck with 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.59
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5024	Dual, 1.2 A buck with 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5033	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Mode pin, two enable pins	16-ball WLCSP	1.90
		LDO: 1.7 to 5.5	LDO: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	2 × LDO	300							
ADP5034	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP 28-lead TSSOP	1.99
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5133 ***New***	Dual, 3 MHz buck regulator	Buck: 2.3 to 5.5	Adj (0.8 to 3.8) or 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Adjustable and fixed outputs	16-ball WLCSP	1.29
ADP5134 ***New***	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.5 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Precision enable pins and power-good pins	24-lead LFCSP	2.09
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5135 ***New***	Triple, 3 MHz buck regulator	Buck: 3.0 to 5.5	Adj (0.8 to 3.8)	3 × buck	1800	—	—	—	—	Precision enable pins and power-good pins	24-lead LFCSP	1.69
ADP5037	Dual, 3 MHz, 800 mA buck regulator with dual 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.69
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5040	3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	—	—	—	Individual enable pins, mode pin	20-lead LFCSP	1.39
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5041	3 MHz buck regulator with dual LDO, supervisor, and watchdog timer	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	0.5 (adj)	20, 140	102, 1600	Individual enable pins and supervisor, WDI, mode pin, and MR pin	20-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5070 ***New***	Dual dc-to-dc with boost and inverter outputs for generating V_{POS} and V_{NEG}	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39	1 × boost	Input current limit: boost: 1 A, inverter: 0.6 A	—	—	—	—	Individual enable pins, adjustable outputs, soft start and slew rate	20-lead LFCSP 20-lead TSSOP	2.19
			Inverter: –0.5 V to –39 V below V_{IN}	1 × inverter								
ADP5071 ***New***	Dual dc-to-dc with boost and inverter outputs for generating V_{POS} and V_{NEG}	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39	1 × boost	Input current limit: boost: 2 A, inverter: 1.2 A	—	—	—	—	Individual enable pins, adjustable outputs, soft start and slew rate	20-lead LFCSP 20-lead TSSOP	2.39
			Inverter: –0.5 V to –39 V below V_{IN}	1 × inverter								
ADP320	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3; LDO2: 1.8, 3.3; LDO3: 1.5	3 × LDO	200	—	—	—	—	Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP322	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3, 2.8, 2.5; LDO2: 2.8, 2.5, 1.8; LDO3: 1.8, 1.5, 1.2	3 × LDO	200					Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP323	Triple, 200 mA LDO	1.8 to 5.5	Adj (0.5 to 5)	3 × LDO	200	—	—	—	—	Adjustable V_{OUT} options	16-lead LFCSP	0.54
ADP5050 ***New***	Quad buck regulator with LDO with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	—	—	—	I²C interface with individual precision enable pins and power good	48-lead LFCSP	4.39
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5051 ***New***	Quad buck regulator, POR, and WDI with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	I²C interface with individual precision enable pins and power good	48-lead LFCSP	4.59
				2 × buck	1200							
ADP5052 ***New***	Quad buck regulator with LDO	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	—	—	—	Individual precision enable pins with power good	48-lead LFCSP	3.59
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5053 ***New***	Quad buck regulator with POR and WDI	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	Individual precision enable pins with power good	48-lead LFCSP	3.79
				2 × buck	1200							
ADP5054 ***New***	Quad buck regulator	Buck: 4.5 to 15.5	0.8 to 0.85 × V_{IN}	2 × buck	6000[2]	—	—	—	—	Individual precision enable pins with power good	48-lead LFCSP	4.29
				2 × buck	2500							

[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).
[2] Resistor programmable current limit (6 A, 4 A, or 2 A).

ADIsim Power Design Center—Select, Design, and Simulate with ADIsimPower Tools

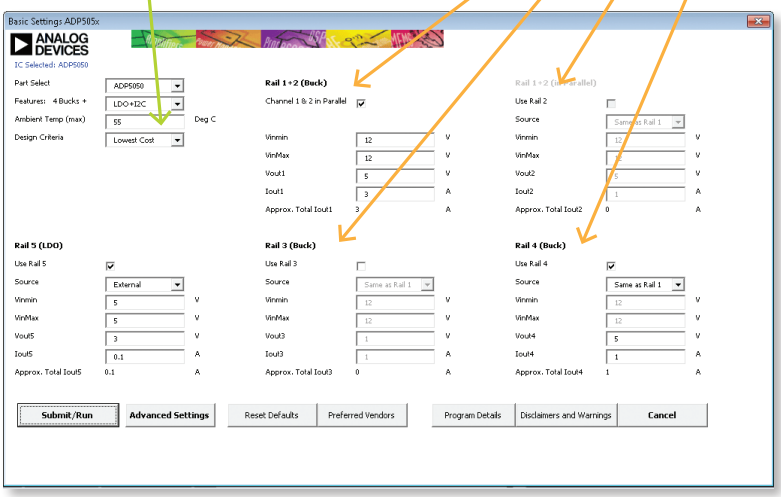
ADP505x Design Tool

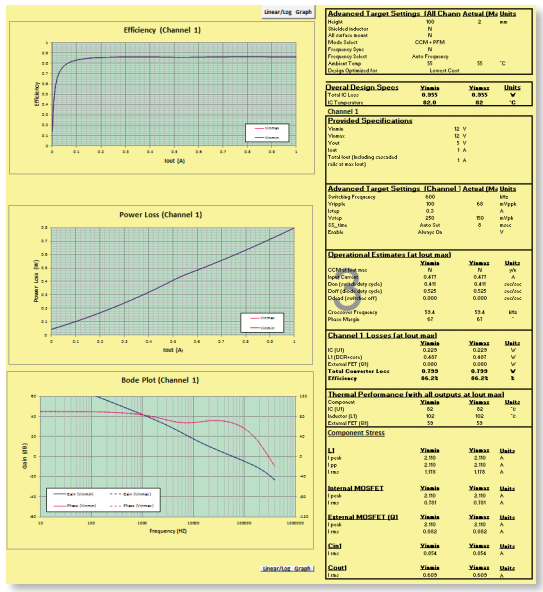
ADIsimPower now supports the ADP505x family of multichannel high voltage PMUs. This new family of parts supports four or five channels from inputs up to 15 V and with load current up to 4 A per channel. Users can optimize the design by taking into account the thermal contributions of each channel by cascading channels, and even by placing the high current channels in parallel to create an 8 A rail. With the advanced features, users can specify independently each channel's performance from ripple and transient to switching frequency selection from the channels that support half the master frequency. As with all the other tools, evaluation boards are available by requests directly from the tool. Download at *download.analog.com/PMP/ADP505x_BuckDesigner.zip*.



Step 1: Optimize for size, cost, or efficiency

Step 2: Specify each channel's operating conditions, including "do not use"





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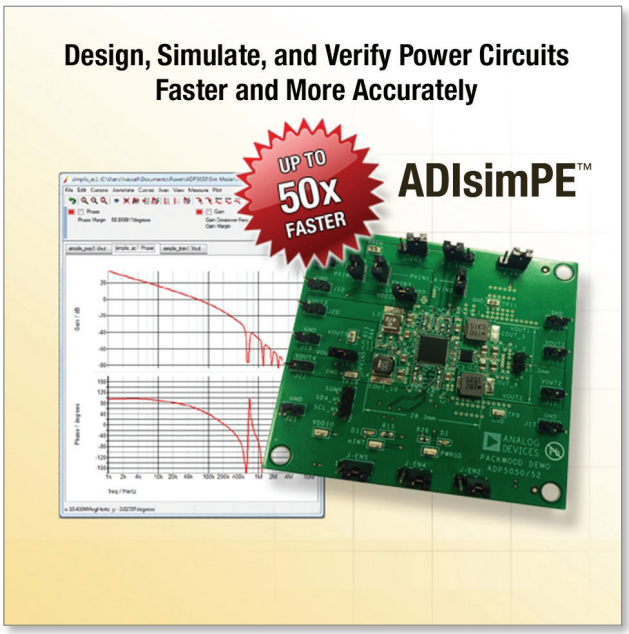

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