OSFP MSA

Specification for

OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

Rev 1.0

March 17th, 2017

Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, mechanical and thermal requirements of the OSFP Module, connector and cage systems. The OSFP Management interface is described in a separate OSFP Management Specification.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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1 Scope

The OSFP specification defines:

- The OSFP module mechanical form factor, including latching mechanism;
- Host cage together with the mating connector;
- Electrical interface, including pin-out, data, control, power and ground signals;
- Mechanical interface, including package outline, front panel and printed circuit board (PCB) layout requirements;
- Thermal requirements and limitations, including heat sink design and airflow;
- Electrostatic discharge (ESD) requirements, and;
- The module management interface (contained in the OSFP Management Specification).

2 References

- IEC 61754-7-1:2014: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 701: Type MPO connector family – One fibre row
- IEC 61754-20:2012: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 20: Type LC connector family.
- CS Connector Specification, Rev0.1, March 10 2017, http://www.qsfp-dd.com/cs-optical-connector/
- SFF-8636: Specification for Management Interface for Cabled Environments, Rev. 2.7 January 26, 2016.
- SFF-8679: Specification for QSFP28 4X Base Electrical Specification, Rev 1.7, August 12, 2014
- UM10204, I^2C-bus specification and user manual, Rev 6 – 4 April 2014
- SFF-8679: Specification for QSFP+ 4X Base Electrical Specification, Rev 1.7 August 12, 2014
- SFF-8024: Specification for SFF Cross Reference to Industry Products, Rev 4.1 June 27, 2016
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
- ANSI/ESDA/JEDEC JS-001-2014: Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level
- IEEE802.3bs: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation
- IEEE802.3cd: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation
- IEEE802.3bj: Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables
- IEEE802.3bm: Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables

3 OSFP Module Mechanical Specification

3.1 Overview

A typical OSFP module is shown in Figure 1. An assortment of connector types are shown.

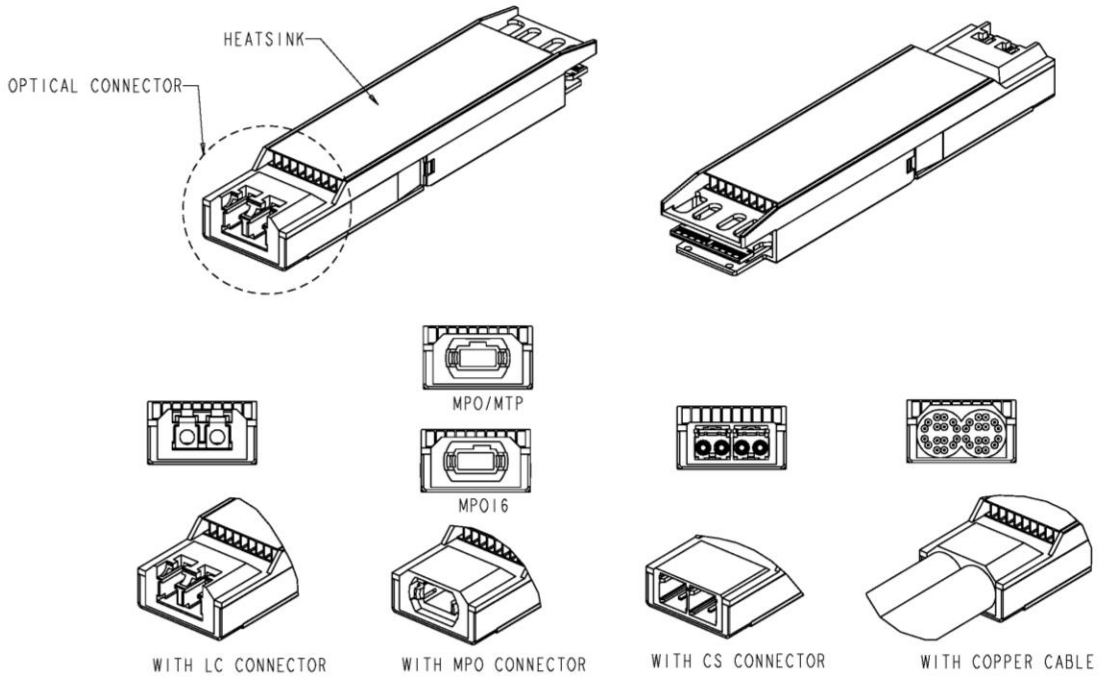


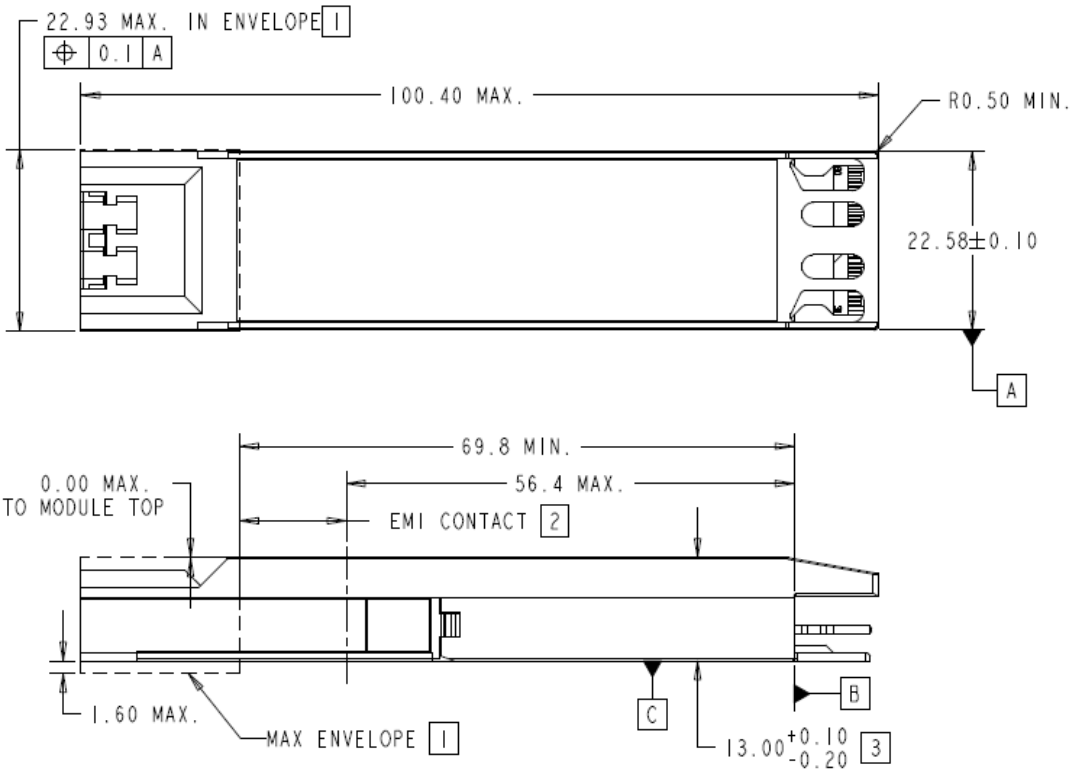
Figure 1: OSFP module with different connectors (Duplex LC, MPO, CS, Copper)

In the module mechanical drawings included throughout this specification, the datum as defined in Table 3-1 shall apply.

Table 3-1: Descriptions of the module mechanical datum

Designator	Description	Figure
A	Width of Module	Figure 2
B	Forward stop of Module	Figure 2; also see Figure 7
C	Bottom surface of Module	Figure 2
D	Width of Module pc board	Figure 17
E	Signal pad leading edge of Module pc board	Figure 17
F	Top surface of Module pc board	Figure 17

Figure 2 shows the dimensions of the OSFP module, including overall lengths, front envelopes and EMI contact area. Note that the module is shown with a typical latch release mechanism without pull tab. Alternate latch release mechanisms are allowed. All dimensions in this specification are in millimeters (mm) unless otherwise noted.



NOTES:

1 FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.6MM MAX FROM THE BOTTOM OF THE MODULE AND CAN HAVE UP TO 22.93mm WIDTH IN THE MAX ENVELOPE SHOWN.

2 INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

3 APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

Figure 2: OSFP overall dimensions

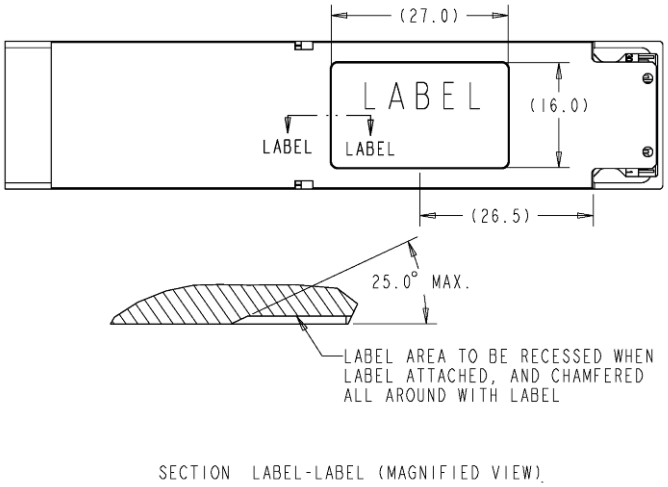


Figure 3: OSFP label reference location

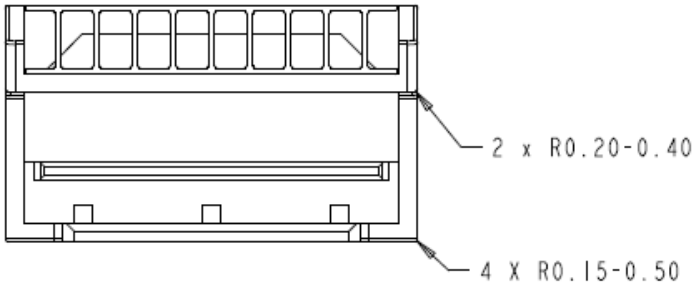


Figure 4: OSFP corner radius

Figure 3 shows the recommended label location. Figure 4 shows the corner radius.

3.2 OSFP Nose

To mate with an electrical connector located in the cage, an OSFP module shall have a protruded printed circuit board (PCB) with contact pads. A structure consisting of upper and lower lips forms a nose (i.e. back of the module) that serves as a guard to protect the PCB. Figure 5 through Figure 11 show the dimensional requirements of the nose, including the shape of the lip, connector mating area, forward stop, ventilation holes and location of the signal pads.

Figure 7 shows the location of the forward stop, consisting of the left and right vertical side walls of the bottom case of the module, which interact with features in the connector cage to stop the module when it is fully inserted. The vertical side walls shall extend at least 7.0 mm upward as measured from the bottom of the module.

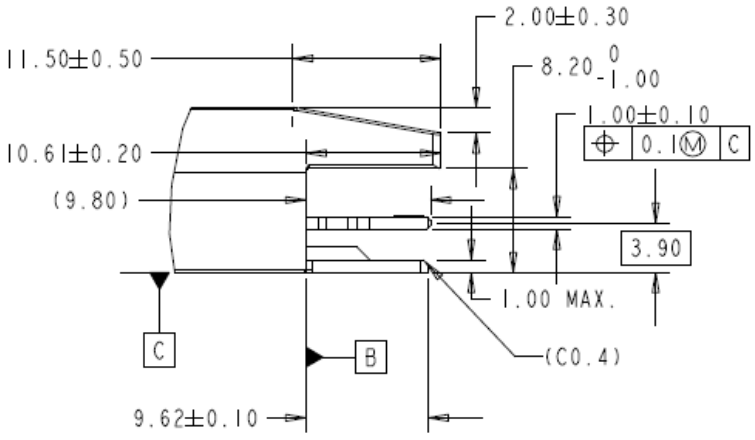


Figure 5: OSFP nose, side view

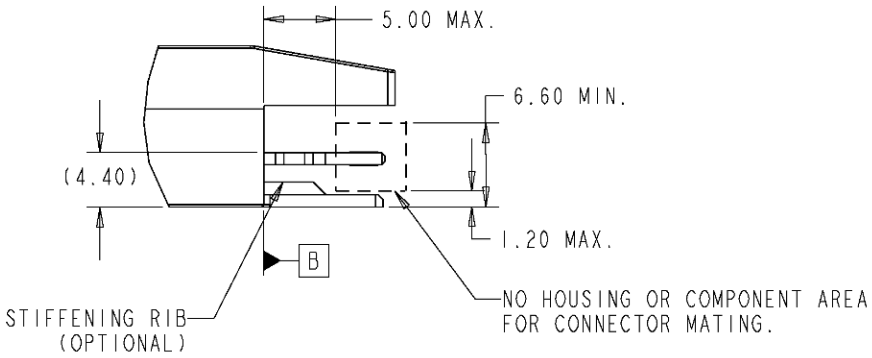


Figure 6: OSFP nose, side view, no component area

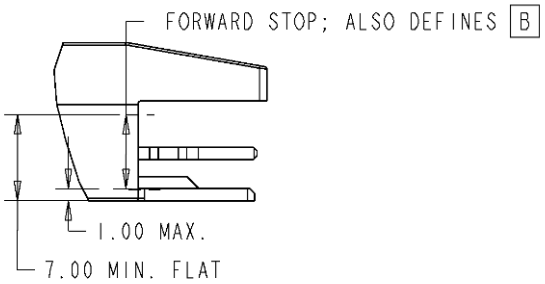


Figure 7: OSFP nose, side view, location of the forward stop

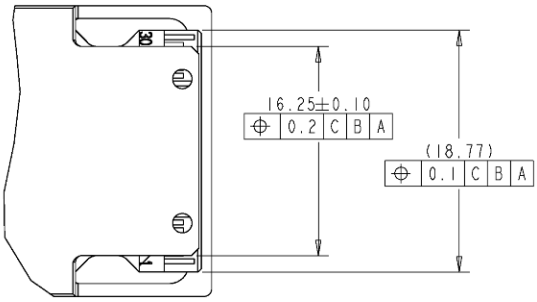


Figure 8: OSFP nose, bottom view

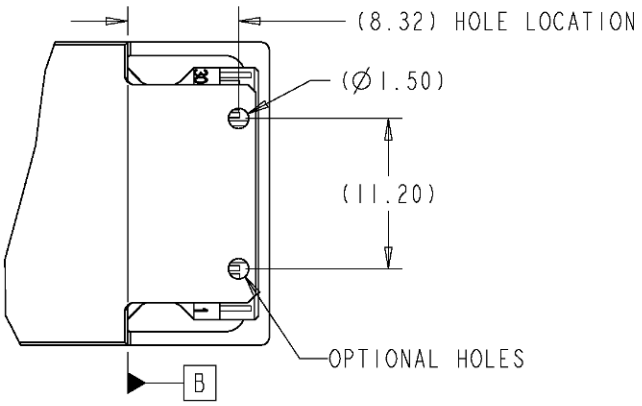


Figure 9: OSFP nose, bottom view, optional signal pad inspection holes

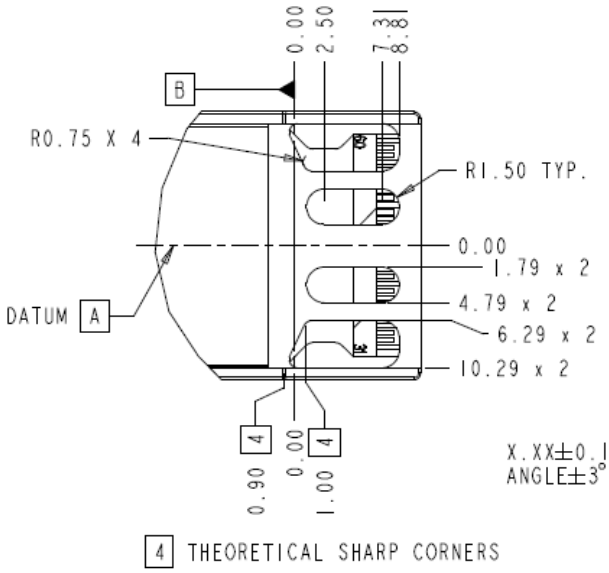


Figure 10: OSFP nose, Top view, Ventilation holes

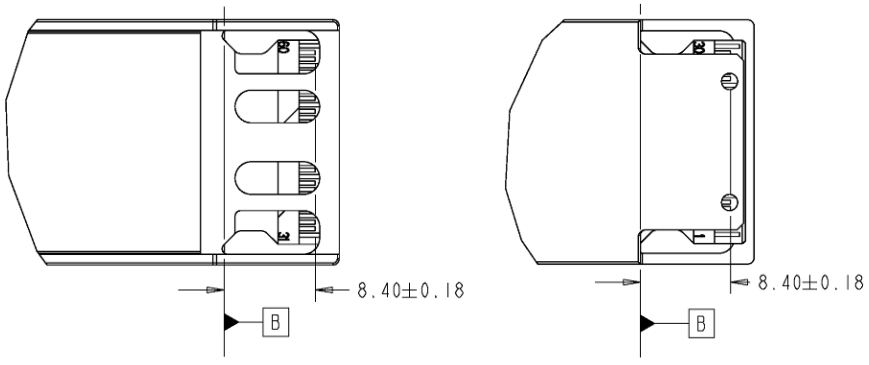


Figure 11: Signal pad location to module (left: top view, right: bottom view)

3.3 Heat Sink, Flat Top

In order to dissipate heat, the module allows for airflow along its length. Figure 12 shows requirements for the heat sink location in order to avoid collision with the keying feature in the cage and also ensure proper contact with ground and an optional thermal interface. Refer to Figure 31 for details of the key feature located in the cage.

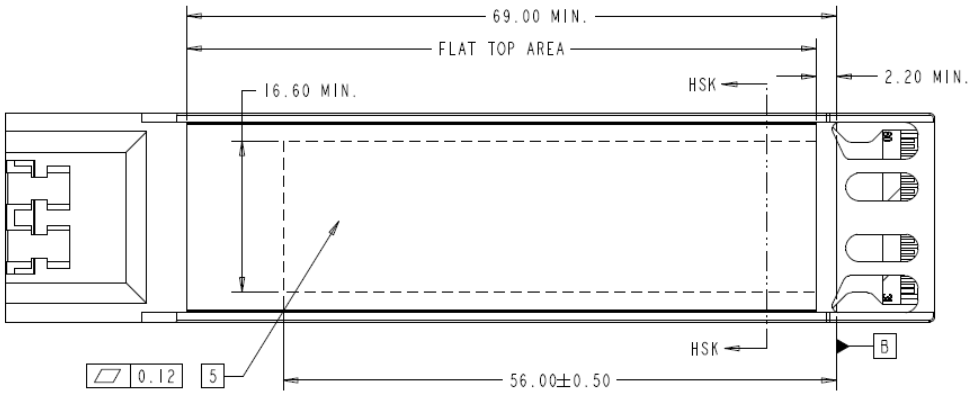


Figure 12: Heat sink, top view

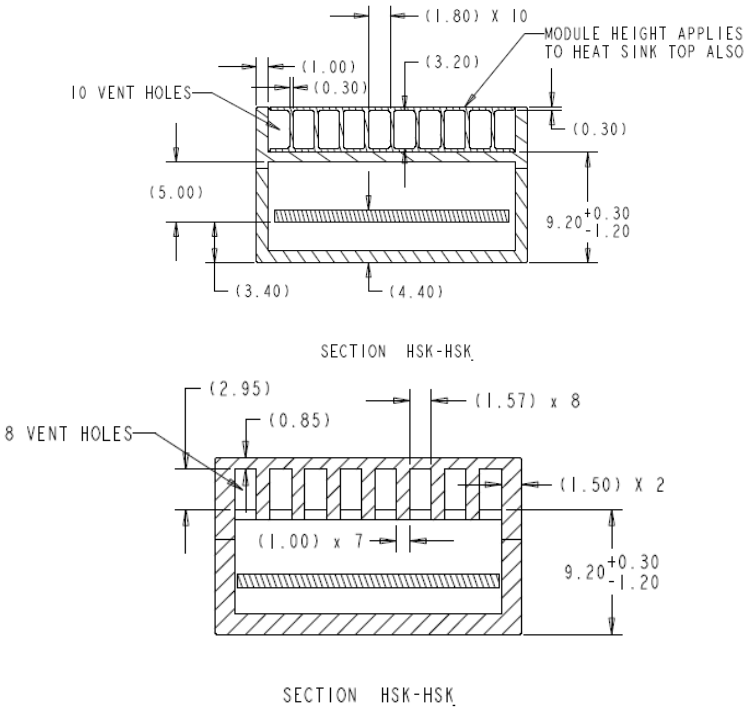


Figure 13. Examples of heat sink design (See Figure 12 for cross-section location)

Figure 13 presents two examples of heat sink design. Either may be considered for use, but any heat sink design should allow for an amount of airflow as defined in Section 6.1.

3.4 Heat Sink, Open Top

Modules which have a non-flat top, i.e. open top, are allowed only when the heat sink fins are designed to meet the dimensional requirements outlined in Figure 14 through Figure 16 in order to prevent EMI finger damage and to ensure proper EMI shielding.

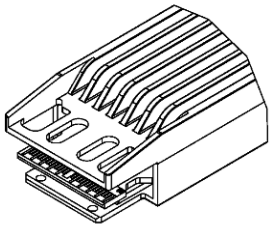


Figure 14. Open top heat sink (Isometric view)

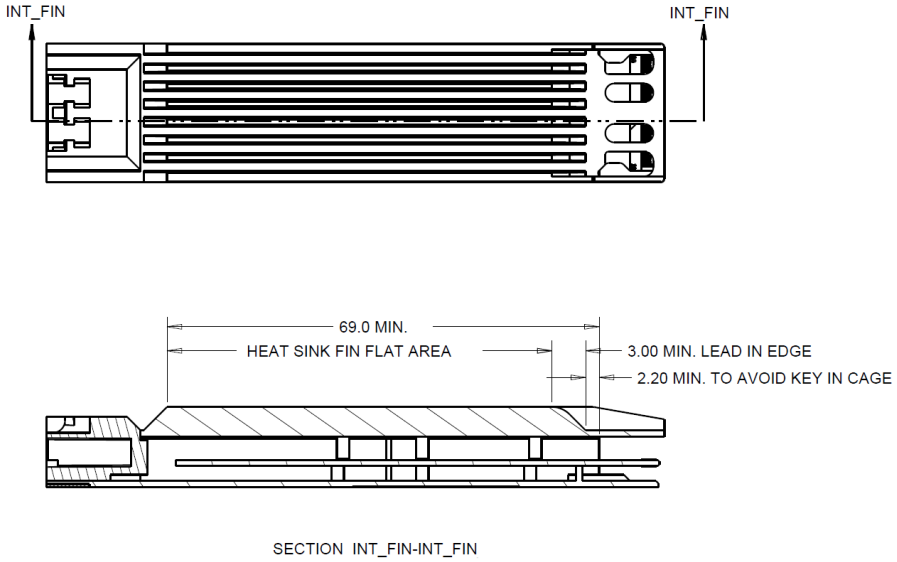


Figure 15. Heat sink location

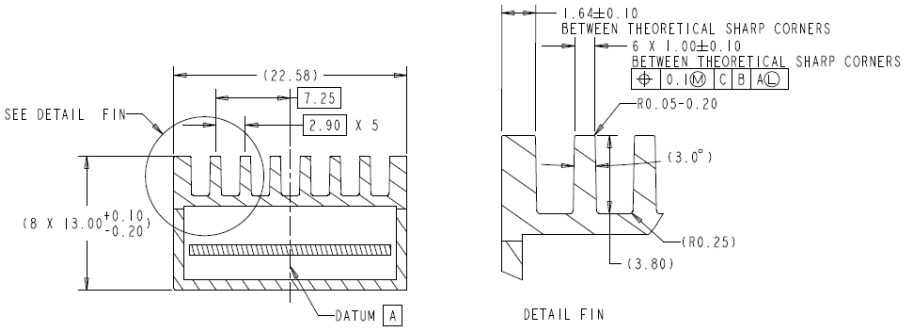


Figure 16. Heat sink fin pitch

3.5 Card-edge Design (Module Electrical Interface)

The OSFP module contains a PCB with contact pads (i.e. module PC board; paddle card) that mate with a connector as specified in Section 4.9 of this document. Critical dimensions for the contact pads are shown in Figure 17 through Figure 19. The contact pads on the PCB are designed for sequence mating during module insertion as follows:

- First mate: ground contacts
- Second mate: power contacts
- Third mate: signal contacts

During module removal, contact disconnects happen in reverse order of the above, e.g. signal contacts break first.

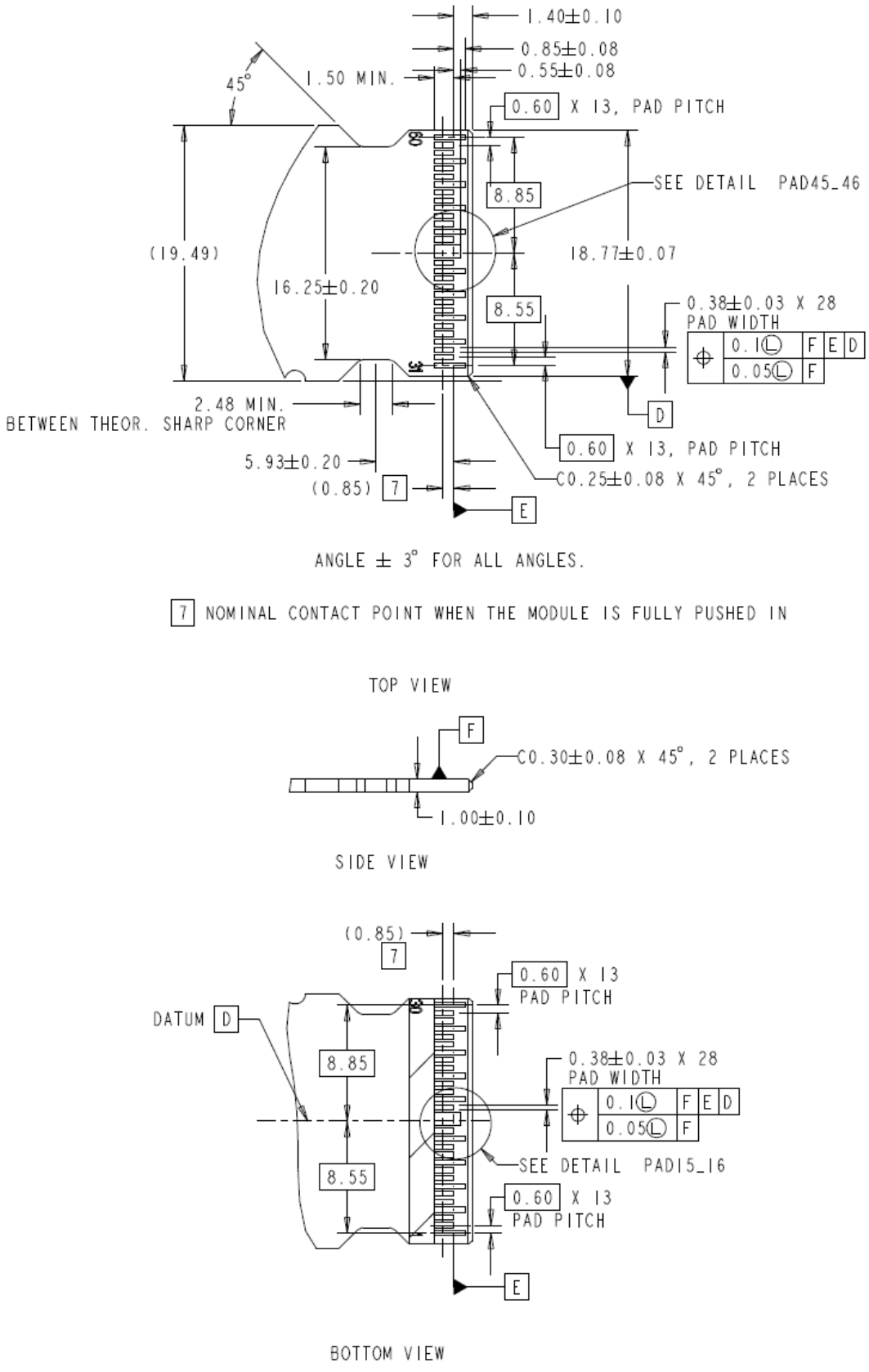


Figure 17: OSFP module pc board (card-edge)

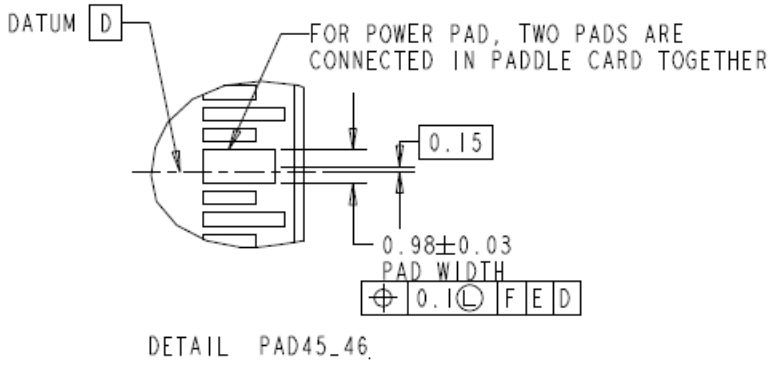


Figure 18: OSFP card-edge, detail of power pad (pads 45/46)

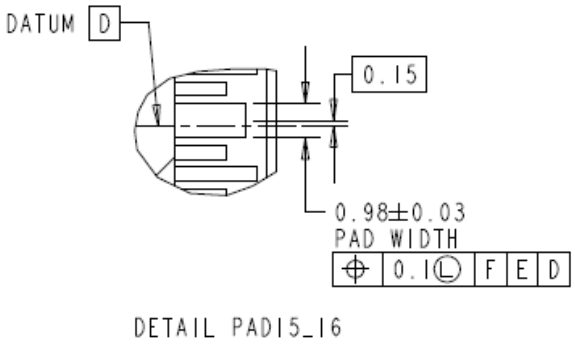


Figure 19: OSFP card-edge, detail of power pad (pads 15/16)

3.6 Contact Pad Plating Requirements

The contact pad plating shall meet the durability requirements of Section 5.1 and Section 5.2. The recommended plating specification is 0.762 µm minimum gold over 3.81 µm minimum nickel. Other plating systems are allowed provided they meet or exceed the requirement of Section 5.1 and 5.2.

3.7 Module Latch Feature

For latching, the module shall have latching pockets and a latch release mechanism at both sides as shown in Figure 20 and Figure 21. Dimensional details of the cage flap can be found in Figure 36 and Figure 37.

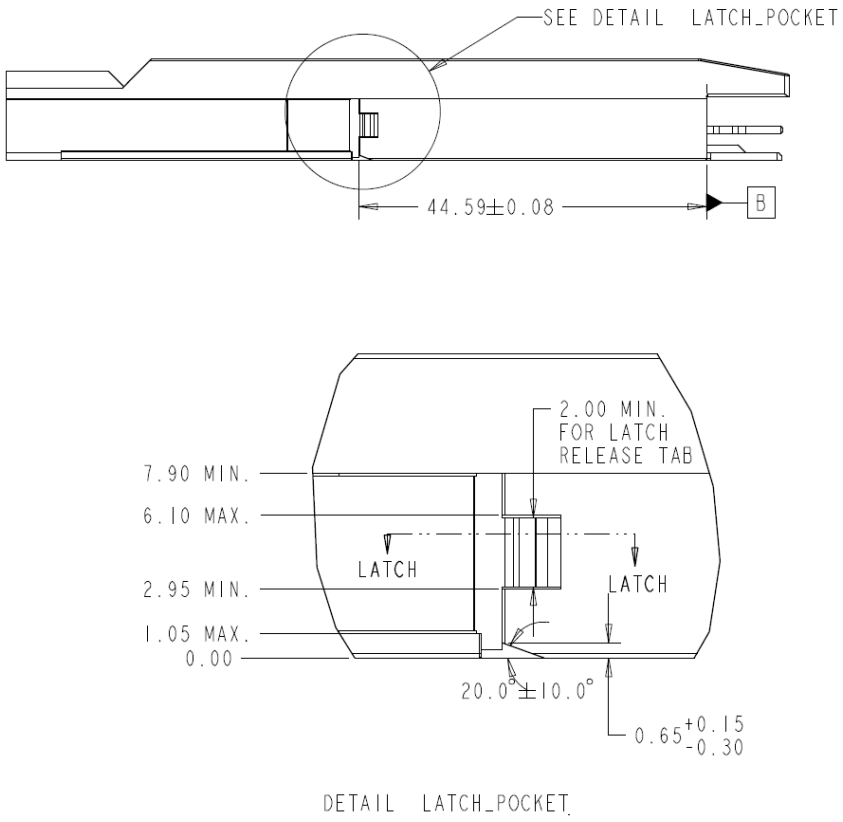


Figure 20. Latch pocket location

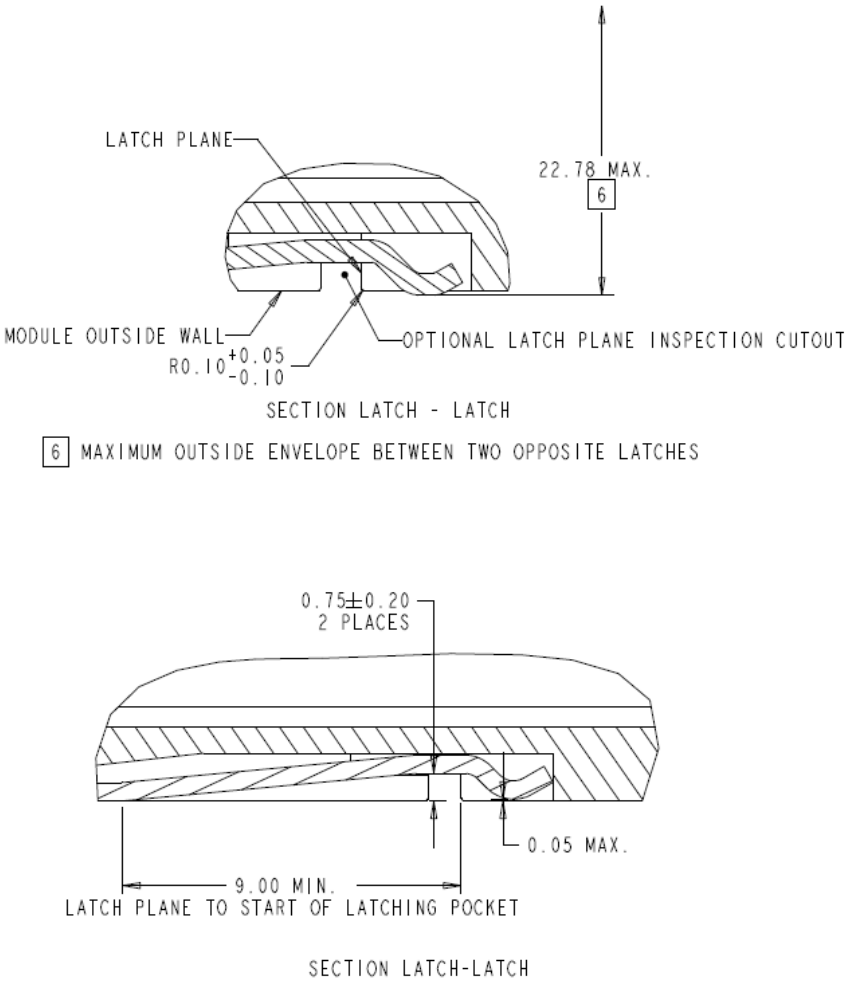


Figure 21: Latch release and latching pocket

3.8 Module Color Code

The module shall adhere to a color code by application of color to its pull-tab or other appropriate method. The color code to be applied is given in Table 3-2.

Table 3-2: OSFP color code

Product Type	Example PMD	Color	Pantone Code (Recommended)
OSFP copper cables	400G-CR8	Black	N/A
OSFP AOC Cables	400G-AOC	Grey	422U
OSFP 850nm solutions	400G-SR8,SR4	Beige	475U
OSFP 1310nm solutions for up to 500m	400G DR4	Yellow	107U
OSFP 1310nm solutions for up to 2km	400G FR4, FR8	Green	354C
OSFP 1310nm solutions for up to 10km	400G LR8	Blue	300U
OSFP 1310nm solutions for up to 40km	400G ER8	Red	1797U
OSFP 1550nm solutions for up to 80km	400G ZR8	White	N/A

4 OSFP Cage and Connector Mechanical Specification

In this section, the configuration of an SMT-type cage and connector is presented.

4.1 Overview

Figure 22 gives an overview of a 1x1 and 1x4 cage without modules installed. Figure 23 depicts a 1x1 cage with an OSFP module in the fully inserted position.

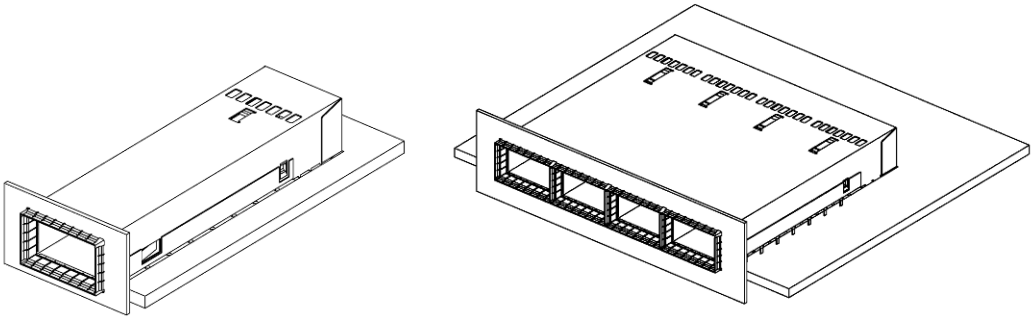


Figure 22: 1x1 and 1x4 Cage, host PCB and panel

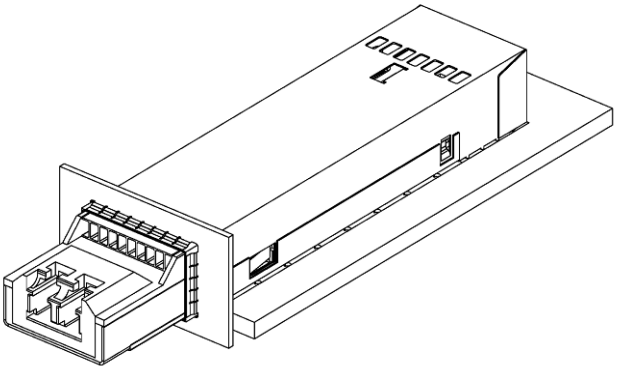


Figure 23: OSFP module in a 1x1 cage

In the cage and connector mechanical drawings included throughout this specification, the datum as defined in Table 4-1 shall apply. For datum of the module, see Table 3-1.

Table 4-1: Descriptions of the cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 24
H	Seating plane of Cage on host pc board	Figure 24
J	Width of inside of Cage	Figure 25
K	Connector guide post #1	Figure 40
L	Cage Pin #1	Figure 24
M	Top surface of host pc board	Figure 32
N	Host pc board through hole #1 to accept Connector guide post	Figure 32
P	Host pc board through hole #2 to accept Connector guide post	Figure 33
R	Host pc board through hole #1 to accept Cage Pin	Figure 33
S	Width of Connector	Figure 40
T	Front surface of Connector	Figure 40
U	Seating plane of Connector	Figure 40

4.2 Cage Dimensions and Positioning Pin

Figure 24 through Figure 27 shows cage datum, positioning pin, port size and cage height. In addition, Figure 28 shows nominal dimensions between the module and the cage when the module is fully inserted.

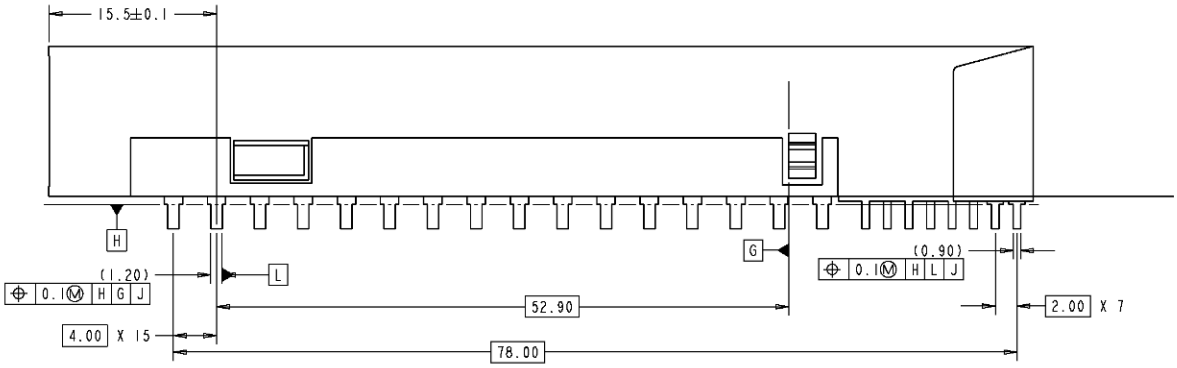


Figure 24. Cage positioning pins and forward stop

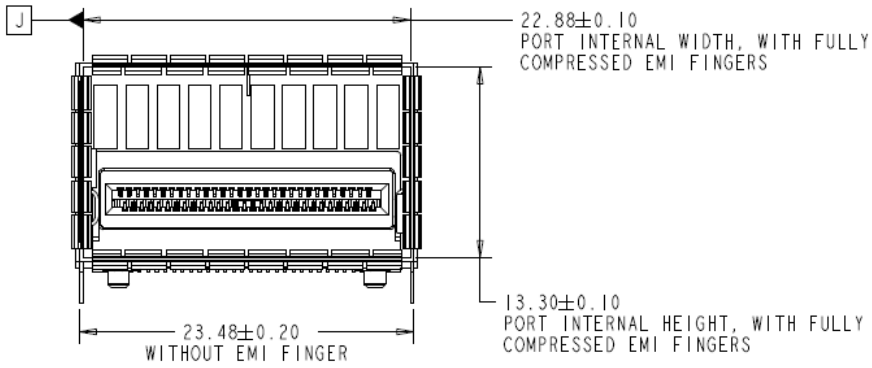


Figure 25: Port internal width and height

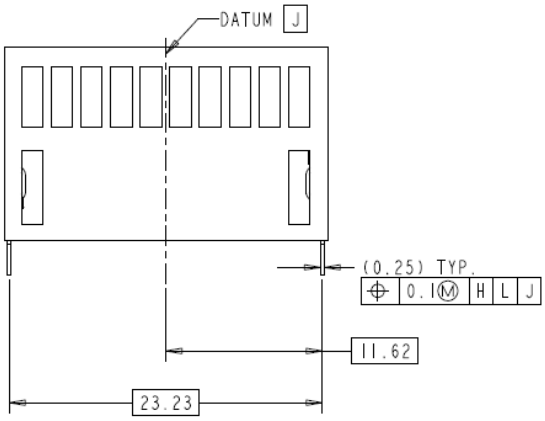


Figure 26. Cage positioning pins

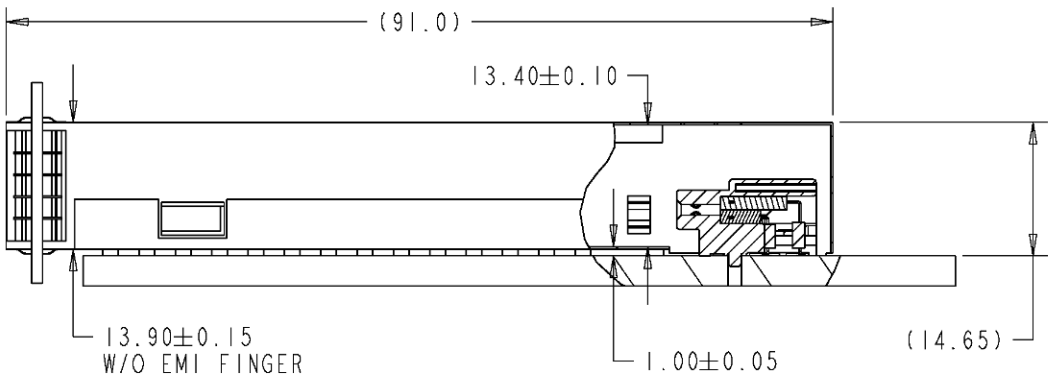
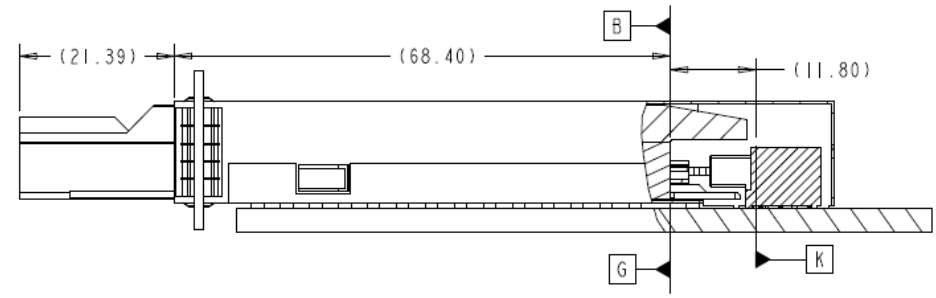


Figure 27: Side view of a 1x1 cage with vertical cage dimensions



DATUM B: MODULE FORWARD STOP
DATUM G: CAGE FORWARD STOP
DATUM K: CONNECTOR GUIDE POST

THIS FIGURE SHOWS THE DATUM ALIGNMENT BETWEEN CONNECTOR, CAGE AND MODULE AND
ALSO SHOWS THE REFERENCE DIMENSION OF THE MODULE INSIDE CAGE, WHEN THE MODULE IS FULLY PUSHED IN.

Figure 28: Side view of a 1x1 cage with axial reference dimensions

4.3 EMI Finger Pitches

Figure 29 gives EMI finger dimensions to be used for the internal side of top and bottom EMI fingers. Fingers for the left, right, and outside of the cage shall be designed to ensure appropriate EMI shielding, but finger pitch is not specified.

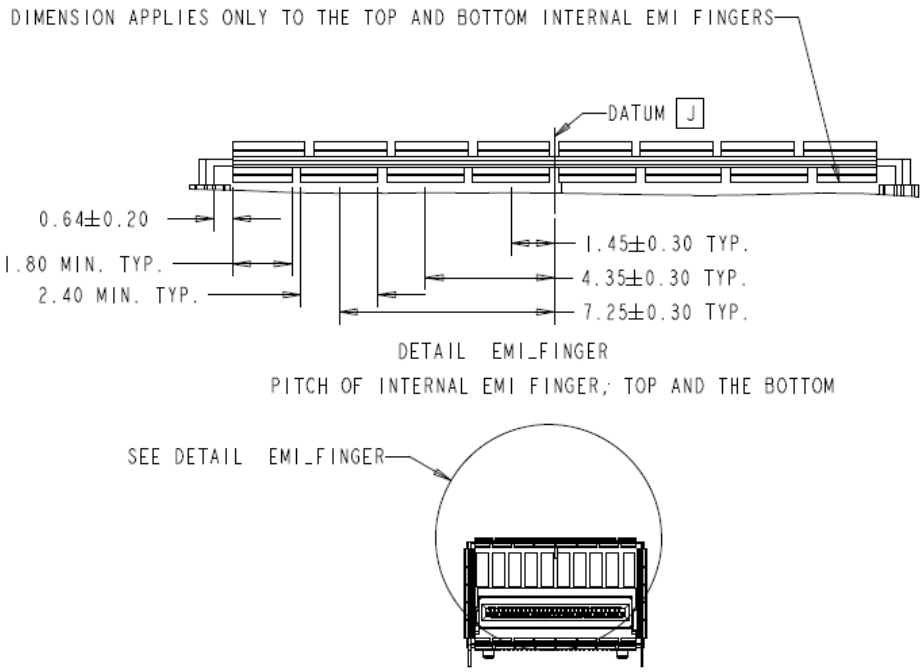


Figure 29. Internal EMI finger, top and bottom

4.4 Ventilation Hole

To allow for forced air cooling of the OSFP module, it is recommended there be ventilation holes in the top and back of the cages. Refer to Figure 30 and Figure 31 for examples of ventilation hole details. Figure 30 shows two different rear ventilation hole designs. The left figure is more conventional, while the right figure shows a variation of the ventilation holes as a single large hole.

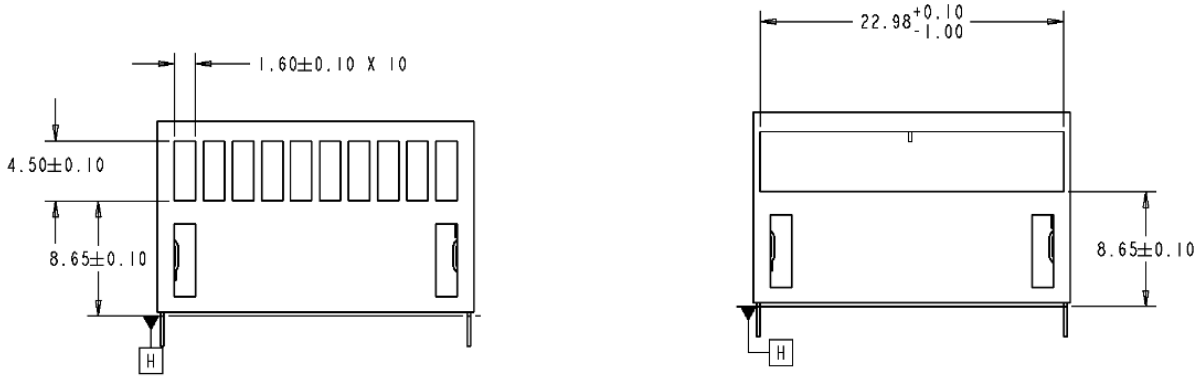


Figure 30: Rear ventilation hole, two example designs

Figure 31 shows the recommended location for ventilation holes (seven are shown) in the top of the cage, along with keying feature and forward stop features. The keying feature is designed to prevent insertion of the module should the module be inserted upside down.

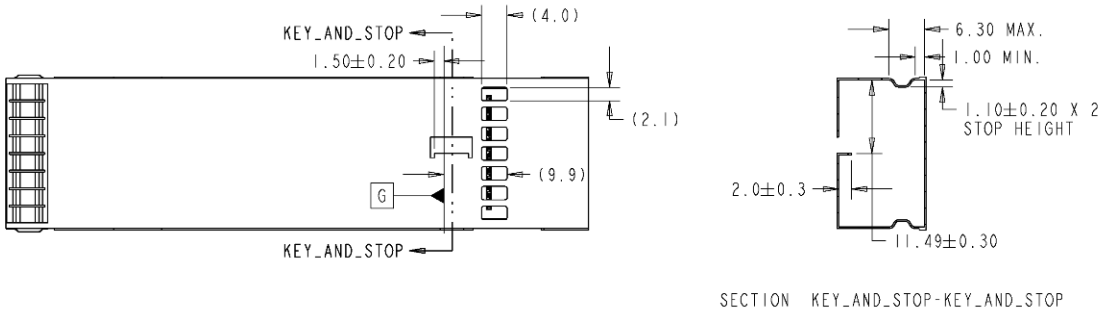


Figure 31: Top vent hole, key and stop

4.5 Host PCB Layout – 1x1 Cage

The host PCB layout pattern to accept a 1x1 cage is detailed in Figure 32 through Figure 34.

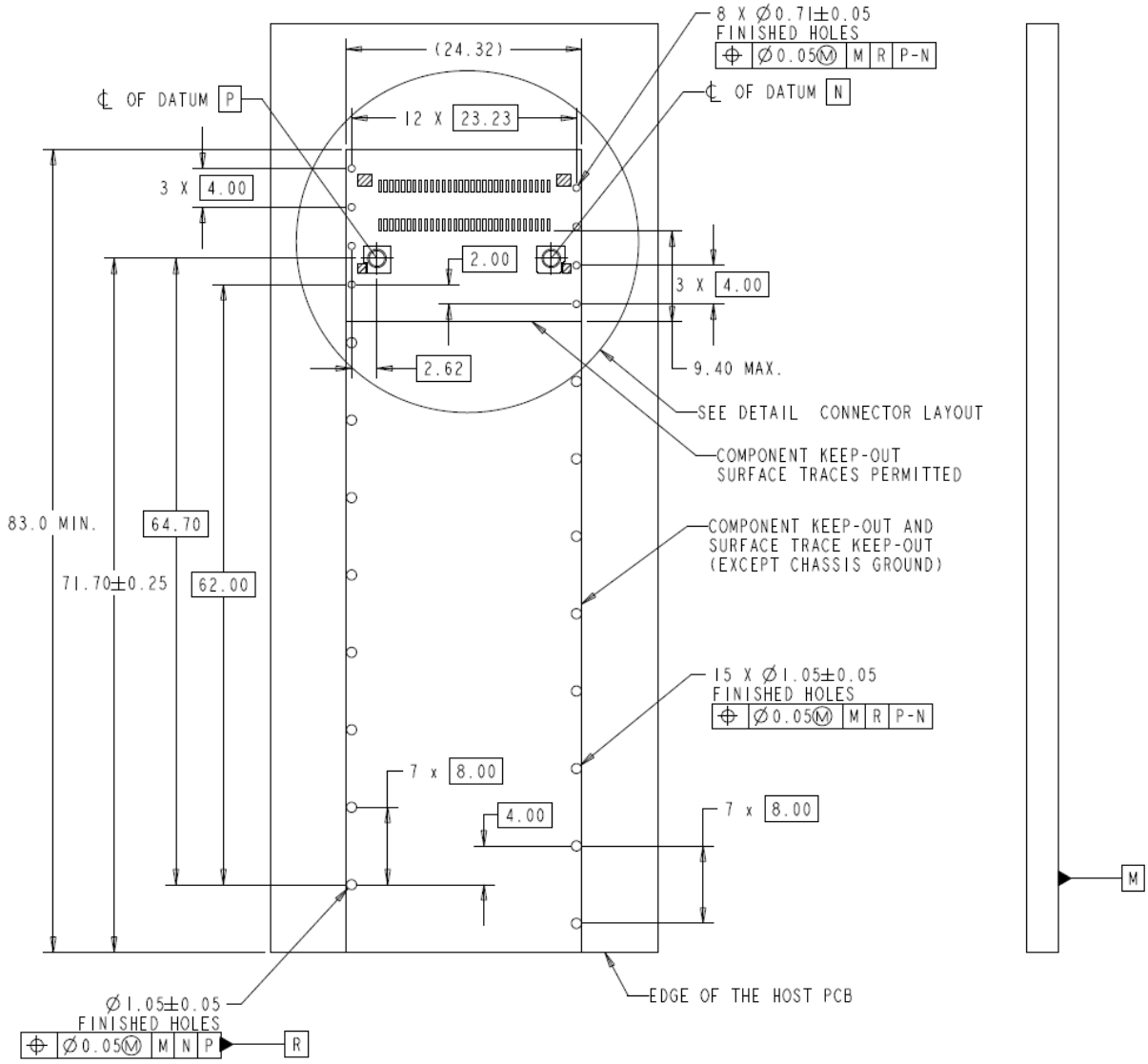


Figure 32: Host PCB layout for 1x1 cage

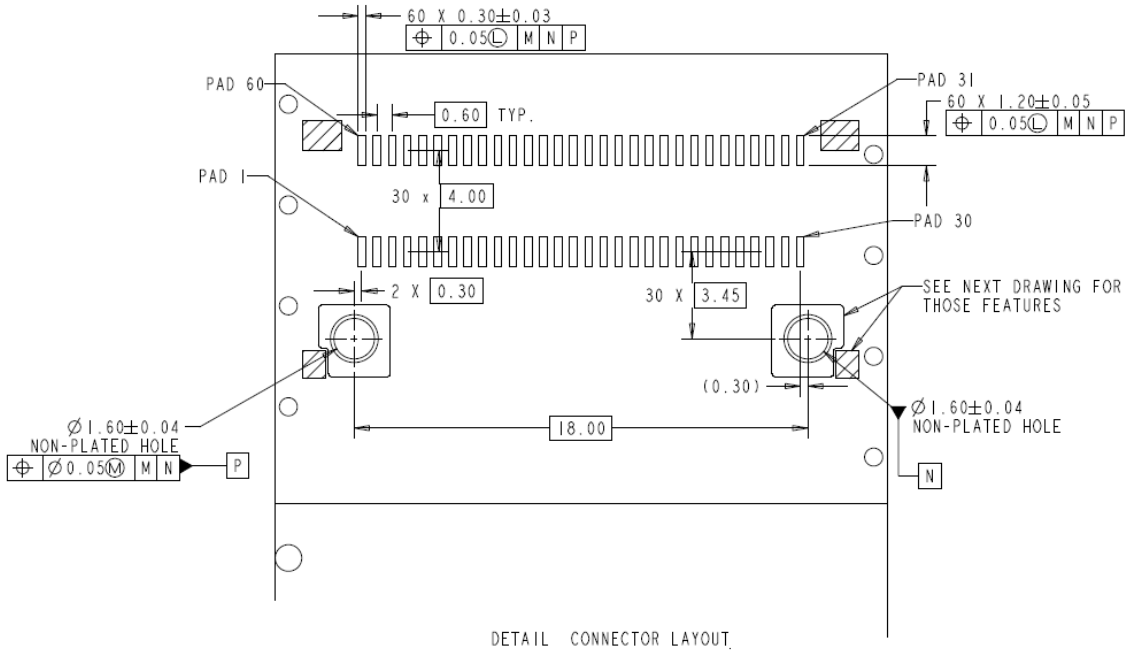


Figure 33. Host PCB layout, details

Figure 34 shows keep out areas and optional solder rings. The solder rings are for SMT belly-to-belly applications, thus applying solder to the area is optional. The keep out areas are there in order to prevent interference with the connector in Figure 40. The keep out areas should be kept in the layout in all cases regardless of whether solder is applied to the optional solder ring area.

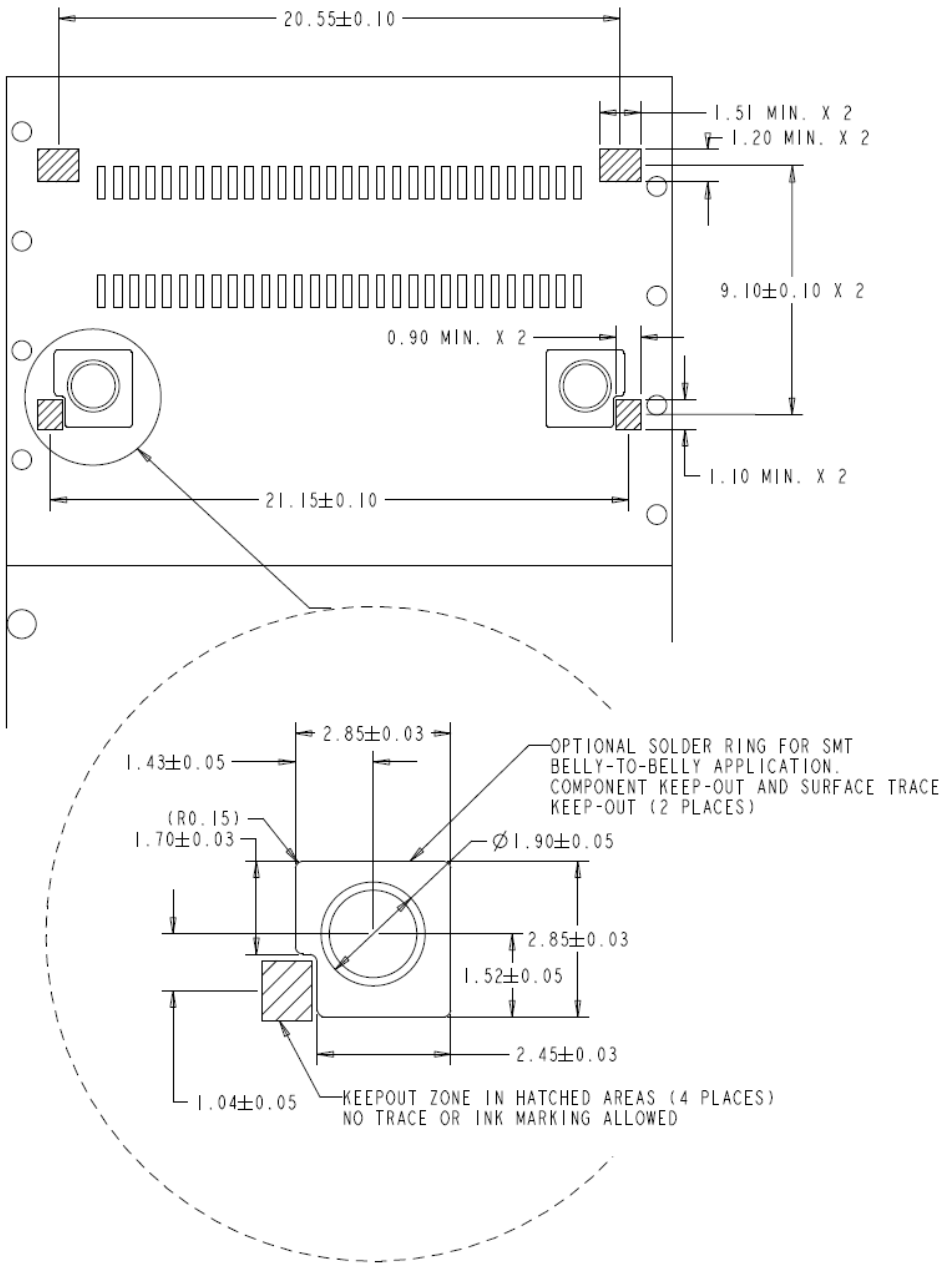


Figure 34. Solder ring for belly-to-belly application

4.6 Host PCB Layout – 1x4 Cage

For a 1x4 cage, the host PCB layout shall have a 23.23mm horizontal pitch from cage-to-cage as in Figure 35.

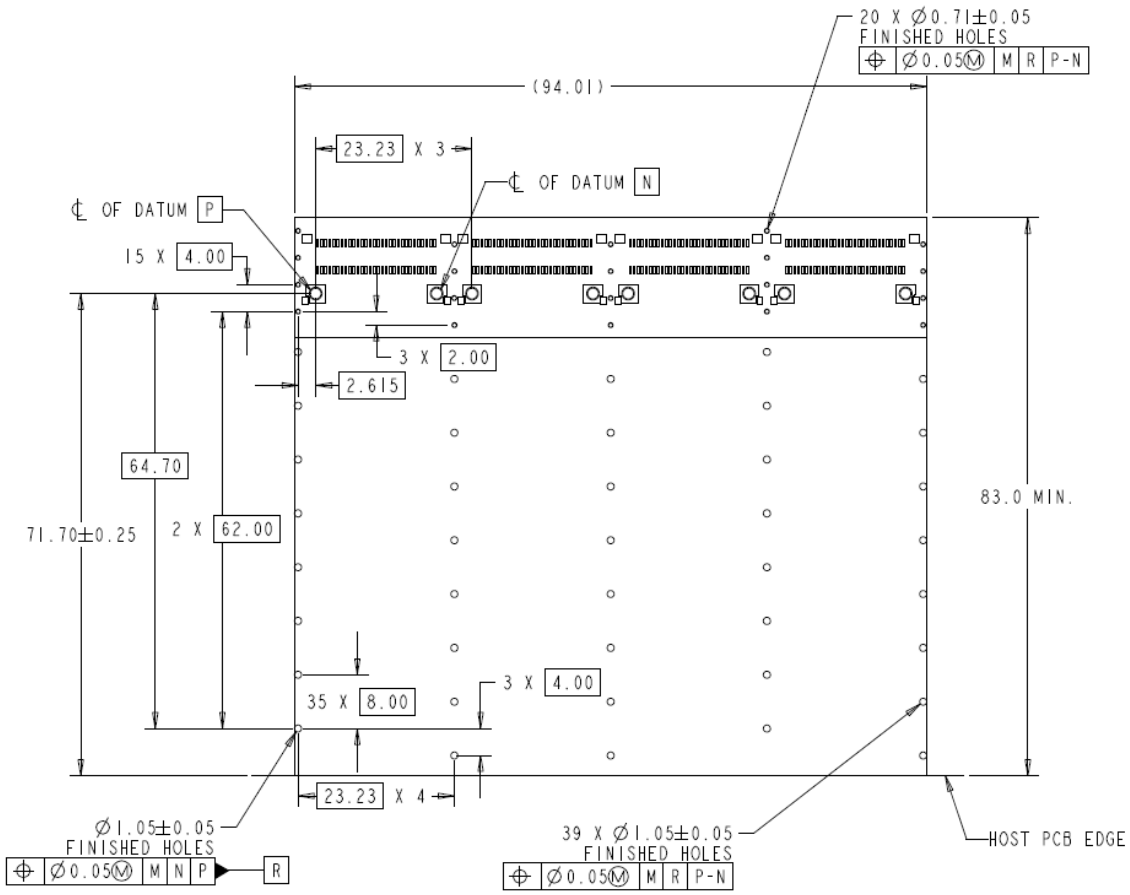


Figure 35: Host PCB layout for 1x4 cage

4.7 Latch Flaps in Cage

In the cage, flaps as shown in Figure 36 and Figure 37 shall be on both sides of the cage to latch the module into the cage. Flaps are shown in a 1x1 cage but can be applied to a ganged cage such as a 1x4 cage or any 1xN cage.

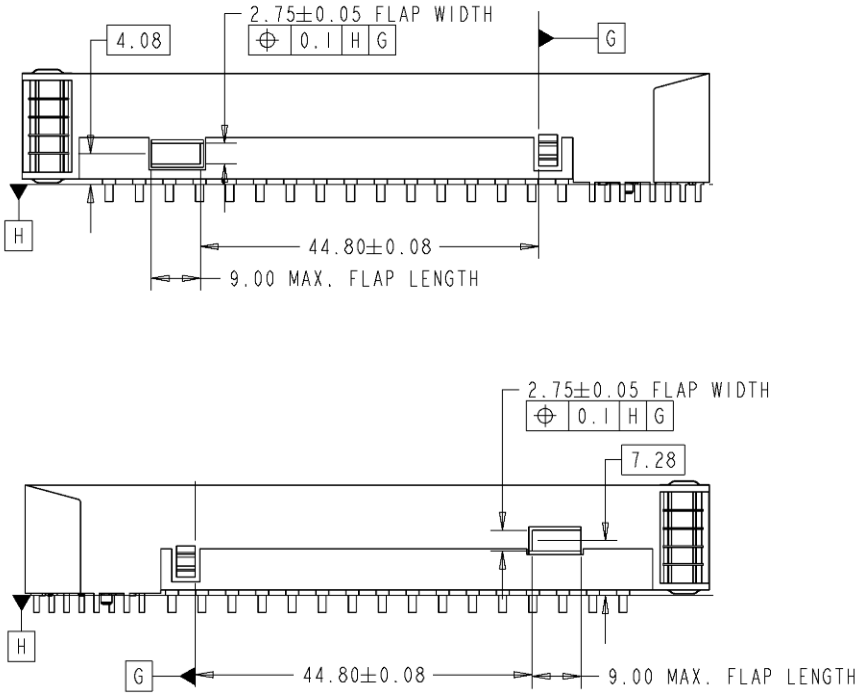


Figure 36: Latch feature, left and right side

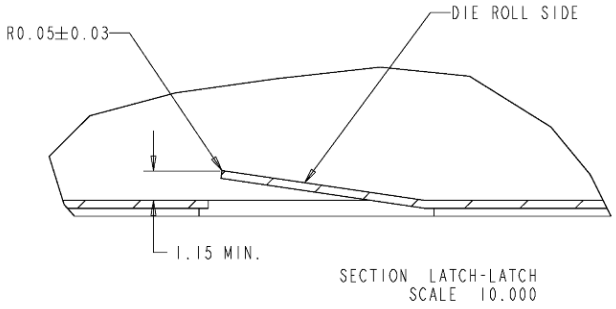


Figure 37: Latch flap, cross-sectional view from top

4.8 Bezel Panel Cut-Out

The EMI spring fingers of the cage shall make contact to the inside of the bezel panel cut out to make ground contact. Figure 38 and Figure 39 show recommended dimensions of the bezel panel cut-out.

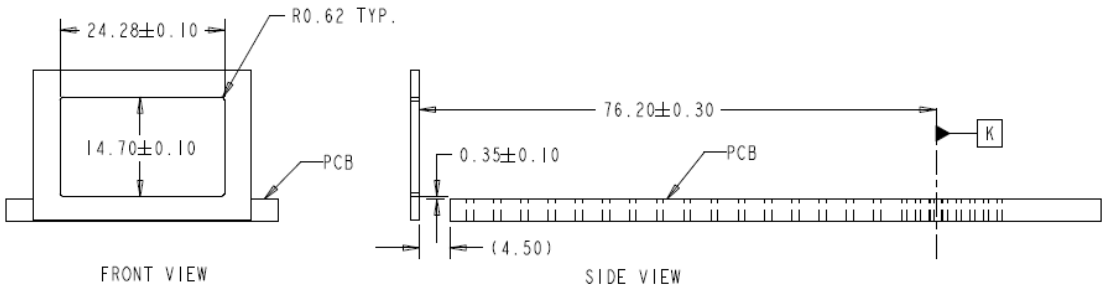


Figure 38: Bezel design and location for 1x1 cage

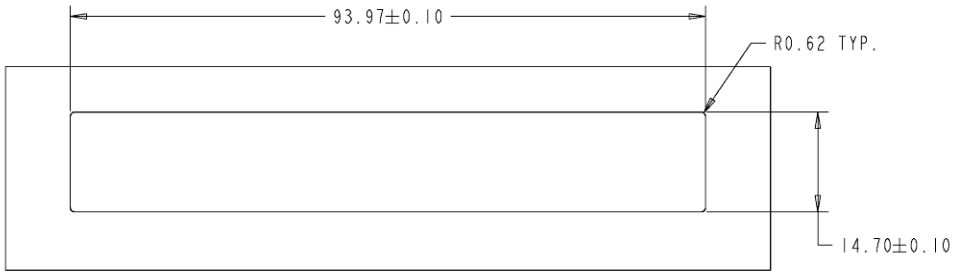


Figure 39: Bezel design for 1x4 cage

4.9 Electrical Connector

The electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module to the outside.

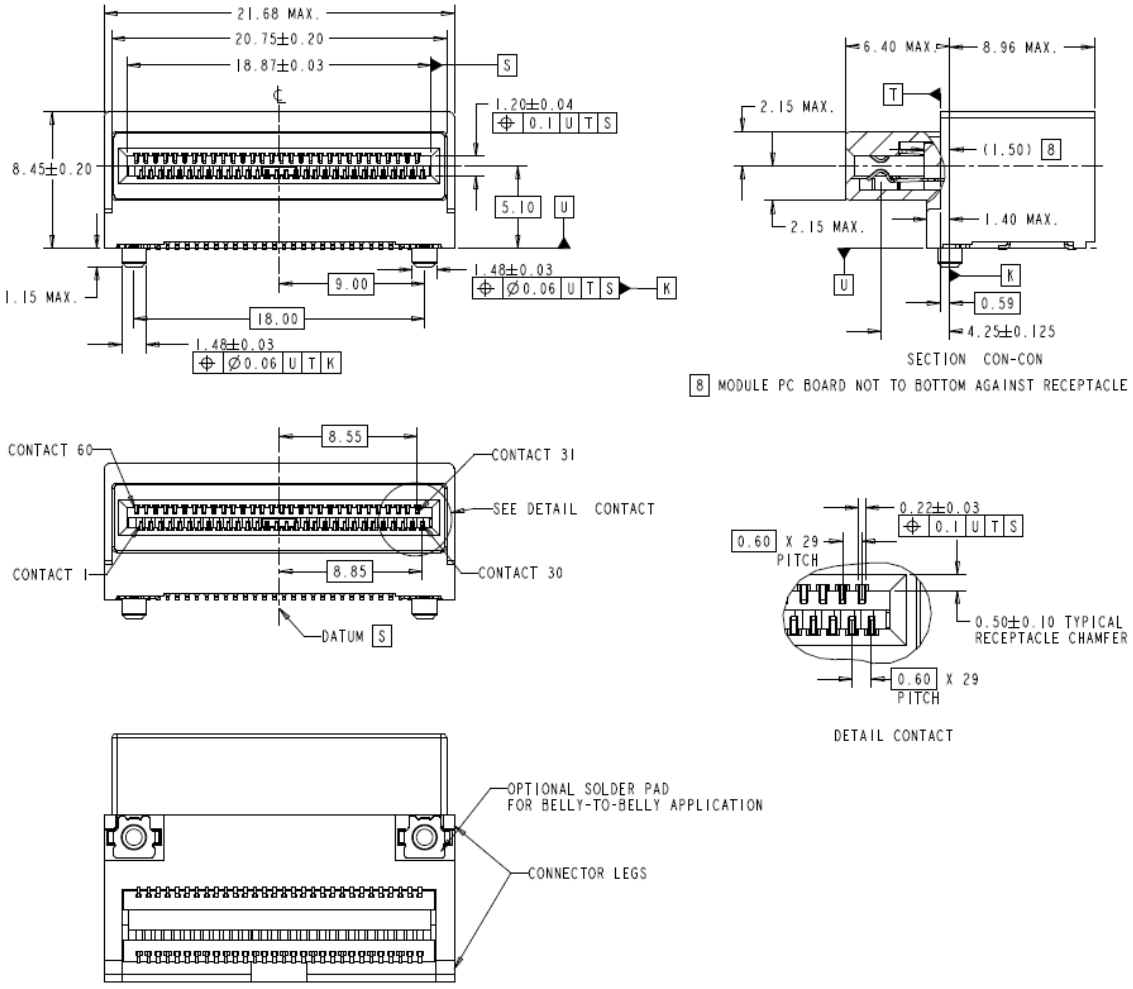


Figure 40: Connector

4.10 Blank Plug

Any unused or empty port of a cage shall have a blank plug. The blank plug shall serve to minimize EMI while at the same time allowing for airflow comparable to a module. See Figure 41 for a recommended design.

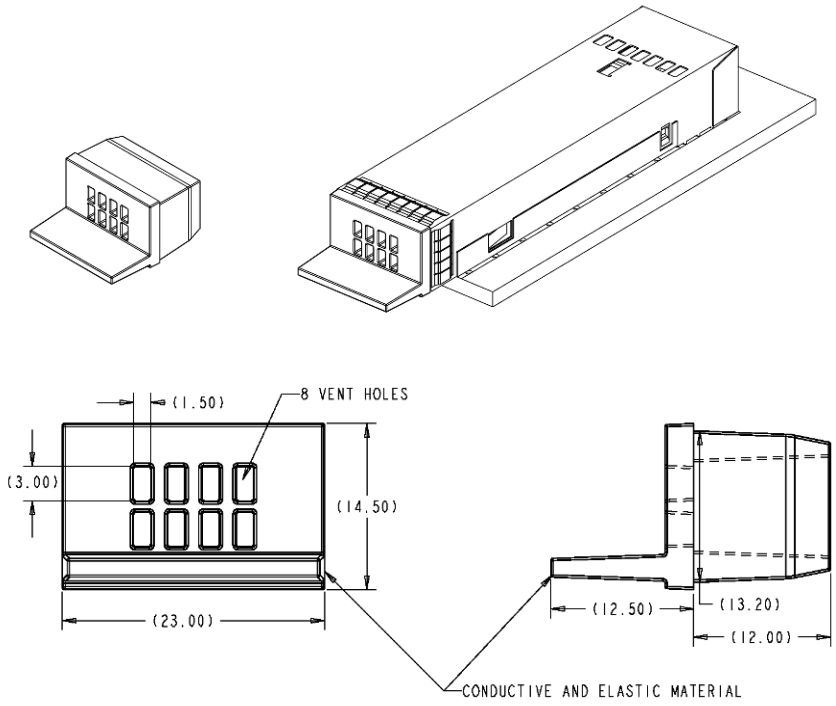


Figure 41: OSFP blank plug (reference design)

5 Plug-in and Removal of an OSFP Module

5.1 Insertion, Extraction, and Retention Forces for an OSFP Module

Table 5-1: Insertion, extraction, and retention forces for an OSFP module

Measurement	Minimum	Maximum	Units	Comments
OSFP Module Insertion	N/A	40	N	Module to be inserted into nominal connector and cage.
OSFP Module Extraction	N/A	30	N	Module to be removed from nominal connector and cage.
OSFP Module Retention in Cage	125	N/A	N	No functional damage to module, connector, or cage.

5.2 Durability

The required number of insertion and removal cycles as applicable to the OSFP module and its mating connector and cage are found in Table 5-2. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 5-2: Durability

Insertion/Removal Cycles into Connector/Cage	Minimum (cycles)	Comments
Module Cycles	50	Number of cycles for an individual module
Connector/Cage Cycles	100	Number of cycles for the connector and cage with multiple module

6 Thermal Performance

6.1 OSFP Module Airflow Impedance Curve

Figure 42 shows a typical airflow impedance range of an OSFP (module only) as measured along or through its heat sink. This typical range of airflow impedance can be used as a reference in an OSFP module's heat sink design and system design.

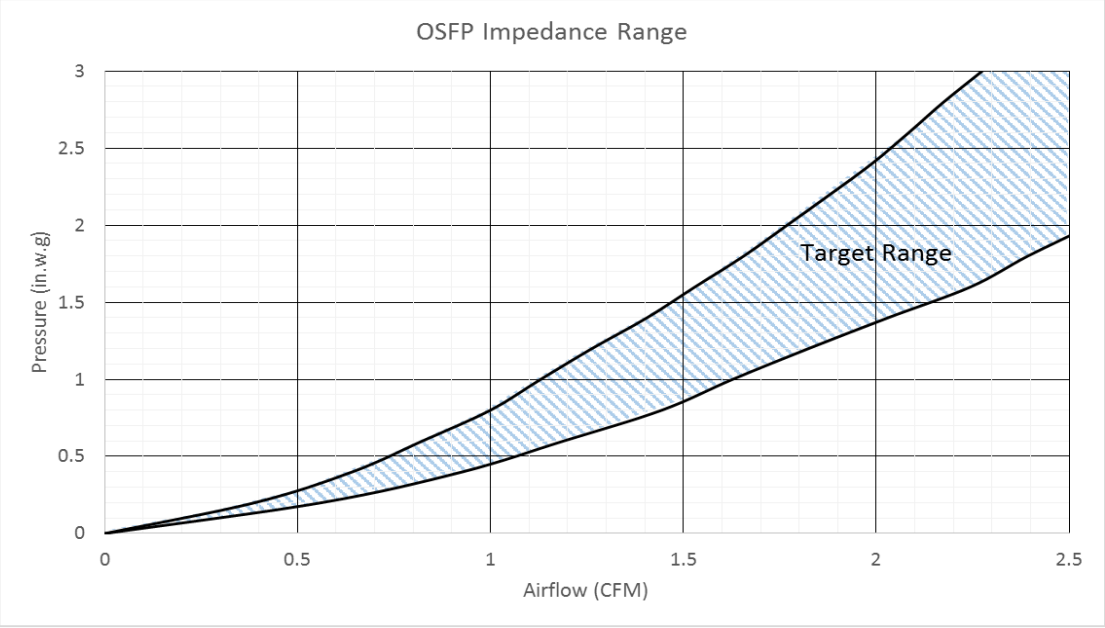


Figure 42: Target range of impediment to airflow of an OSFP module

6.2 Module Airflow Impedance Test Jig

The impedance range of Figure 42 was created using a jig as shown in Figure 43 and Figure 44. The jig is designed to support airflow along the heat sink as well as leakage around the module. A positive stop located within the jig's cavity ensures that the module is inserted into the jig at the same depth as with a cage.

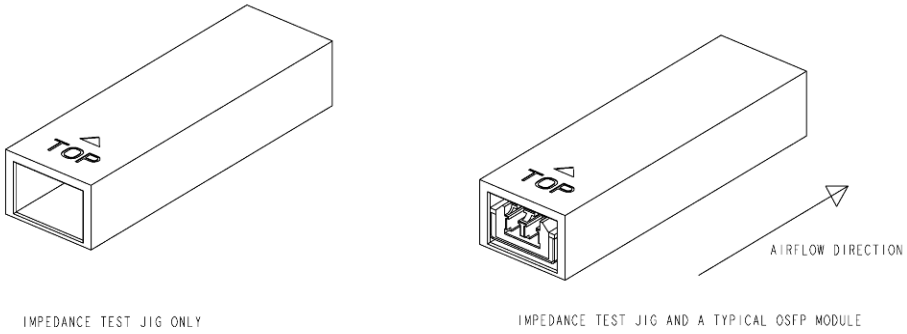


Figure 43: Impedance test setup

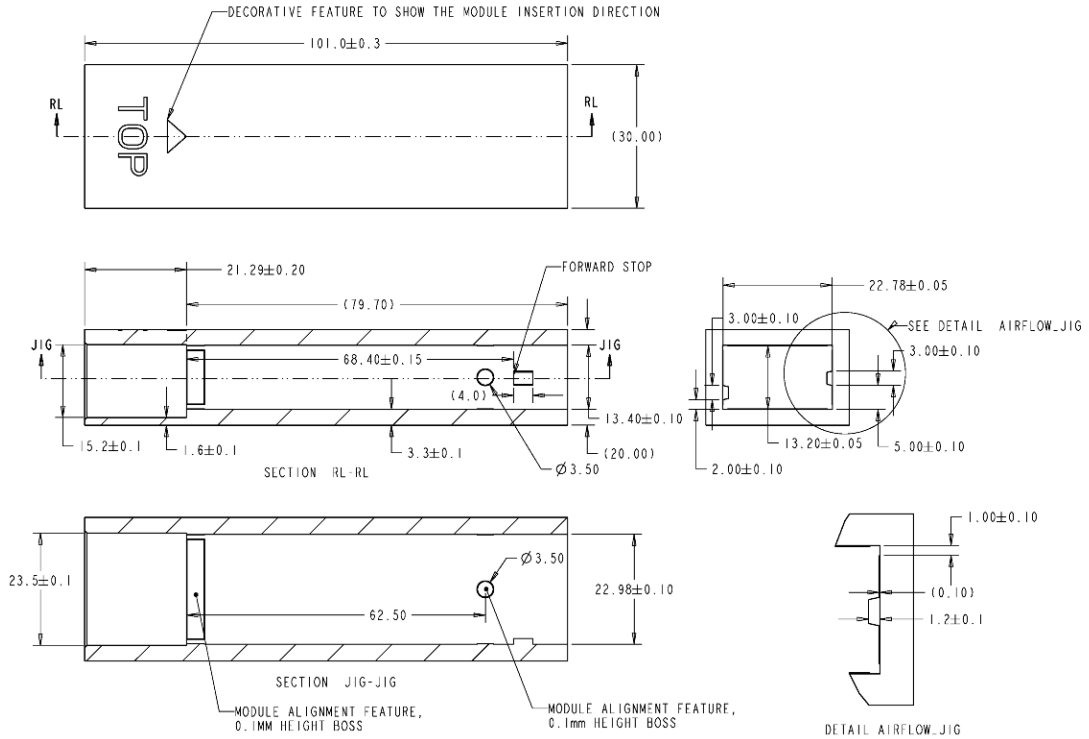


Figure 44: Impedance test jig

7 Optical PMD Block Diagrams

Below sub-sections illustrate block diagrams for a sampling of optical physical medium dependent sublayers (PMDs) that can be realized in an OSFP form factor. These block diagrams are meant to serve as guidelines for better understanding of the form factor and are by no means exhaustive.

7.1 Optical PMD for Parallel Fiber: 400G-PSM4

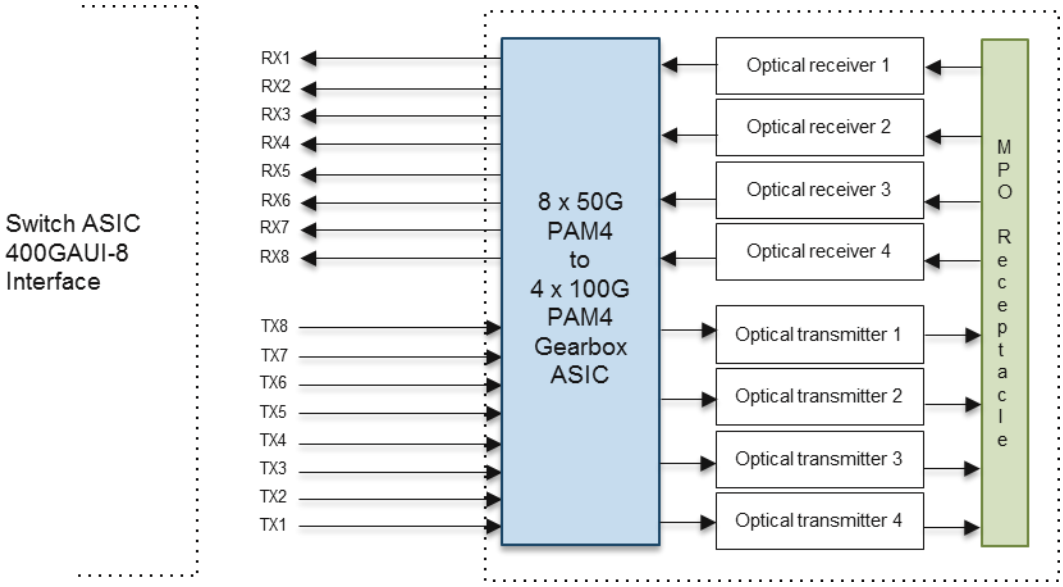


Figure 45: Block diagram for 400G-PSM4

7.2 Optical PMD for Parallel Fiber: 400G SR8

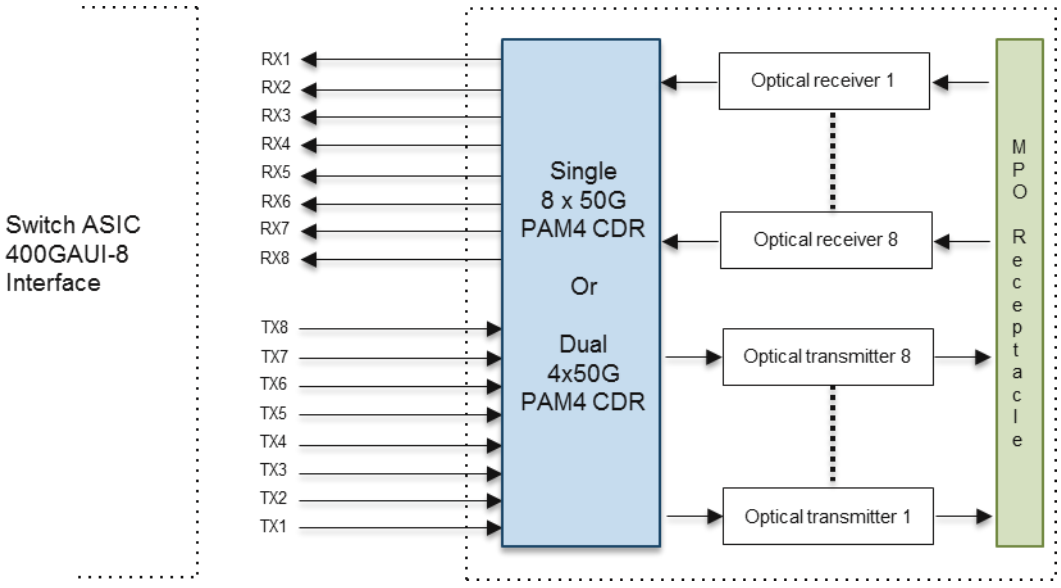


Figure 46: Block diagram for 400G-SR8 (AOC)

7.3 Optical PMD for 400G-FR4, Duplex Fiber

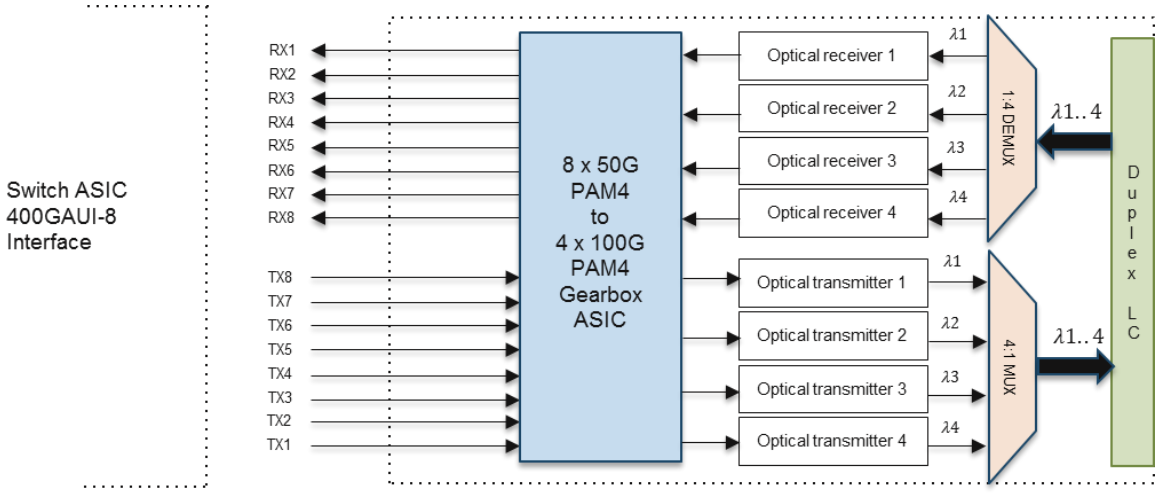


Figure 47: Block diagram for 400G-FR4

7.4 Optical PMD for 400G-FR8/LR8

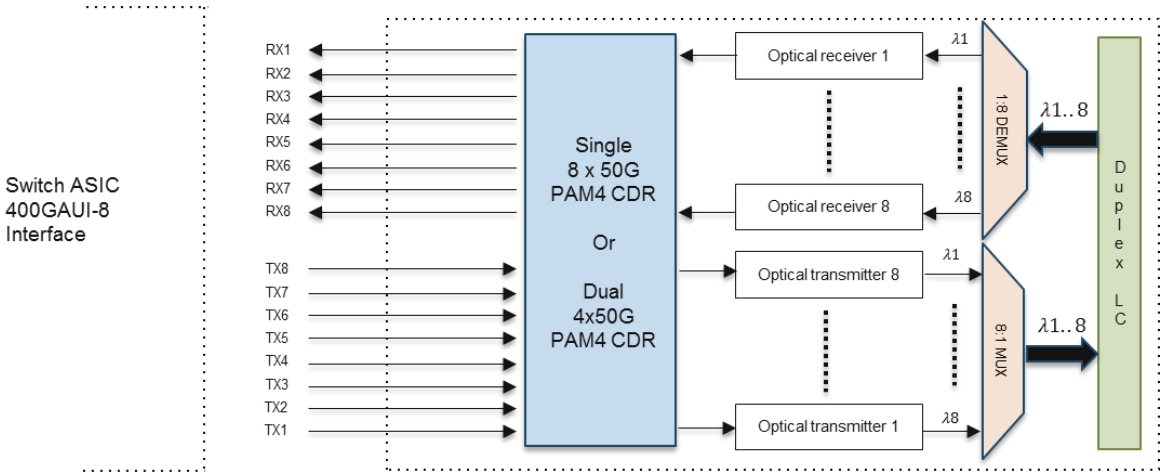


Figure 48: Block diagram for 400G OSFP optical PMD for duplex fiber, e.g. 400G CWDM8, FR8/LR8

7.5 Optical PMD for 2x200G-CWDM4

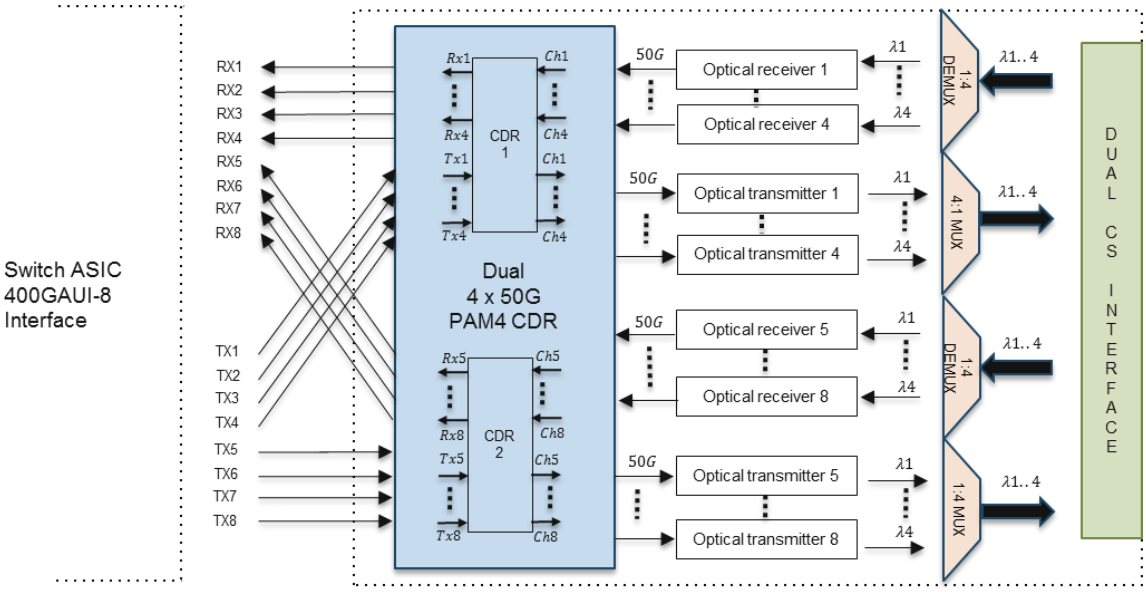


Figure 49: Block diagram for 2x200G-CWDM4

7.6 Optical PMD for 2x100G-CWDM4

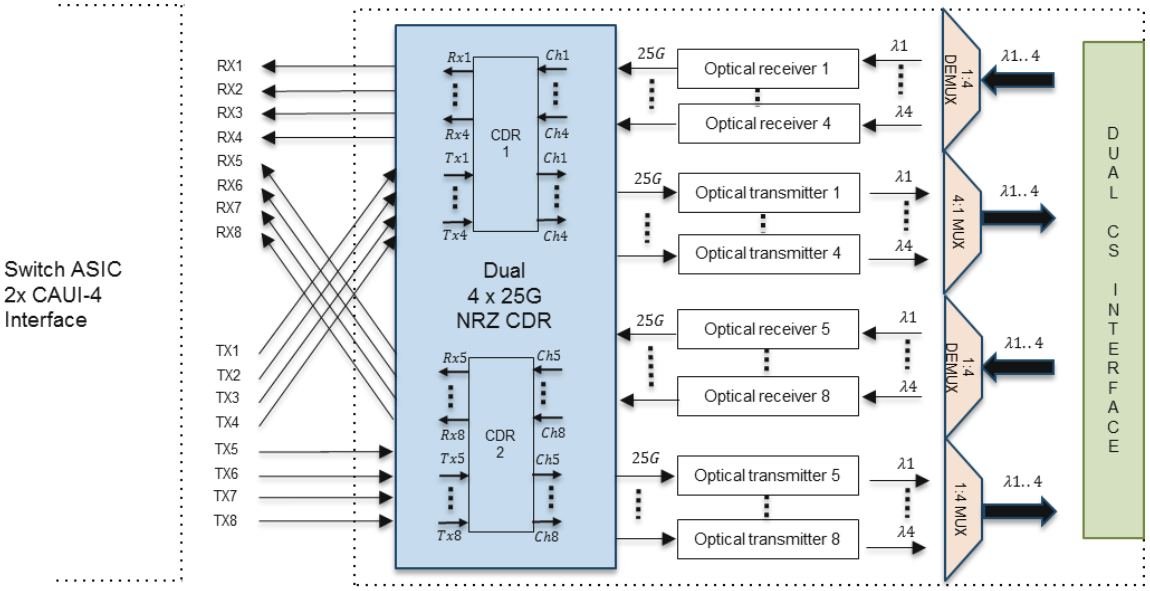


Figure 50: Block diagram for 2×100G-CWDM4

7.7 OSFP Optical Interface

7.7.1 Duplex LC Optical Interface

Figure 51 shows channel orientation of the optical connector when a duplex LC connector as in IEC 61754-20 is used in an OSFP module. The view is from the front of a typical OSFP module, but actual OSFP module design of the heat sink or height of the optical connector may be different than shown.

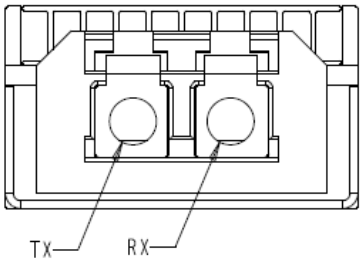
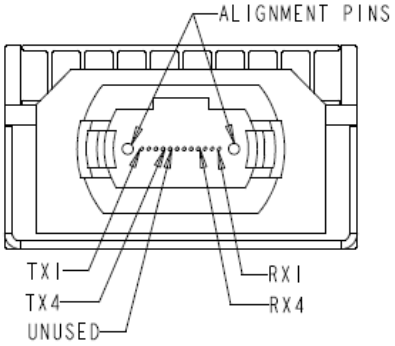


Figure 51. Optical receptacle and channel orientation for duplex LC connector

7.7.2 MPO 12 Optical Interface

Figure 52 shows channel orientation of the optical connector when a male MPO 12 connector as in the IEC 61754-7-1 is used in an OSFP module.

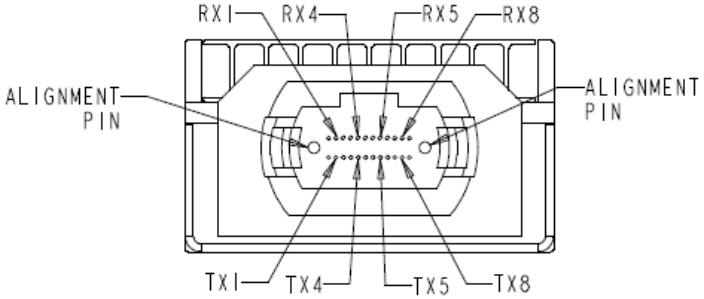


Channels (x: unused position) Tx1 Tx2 Tx3 Tx4 x x x x Rx4 Rx3 Rx2 Rx1

Figure 52. Optical receptacle and channel orientation for MPO 12 connector

7.7.3 MPO 24 Optical Interface

Figure 53 shows channel orientation of the optical connector when a male MPO 24 connector is used in an OSFP module.



Receive Channels x 1 2 3 4 x x 5 6 7 8 x
Transmit Channels x 1 2 3 4 x x 5 6 7 8 x
(x: unused positions)

Figure 53. Optical receptacle and channel orientation for MPO 24 connector

7.7.4 Dual CS Optical Interface

Figure 54 shows channel orientation of the optical connector when a dual CS connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1) and receptacle 2 (Tx2, Rx2) are connected with two separate independent duplex fiber cables.

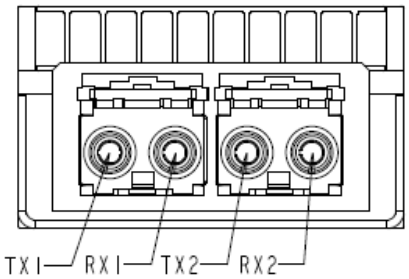


Figure 54. Optical receptacle and channel orientation for dual CS connector

8 Electrical Interface

8.1 Module Electrical Connector

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in Figure 55. It provides 16 contacts for 8 differential pairs of high-speed transmit signals, 16 contacts for 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

The chassis ground (case common) of the OSFP module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module. When an OSFP module is not installed, the signals to the connector within the unused cage should be disabled to minimize electromagnetic interference (EMI) emissions.

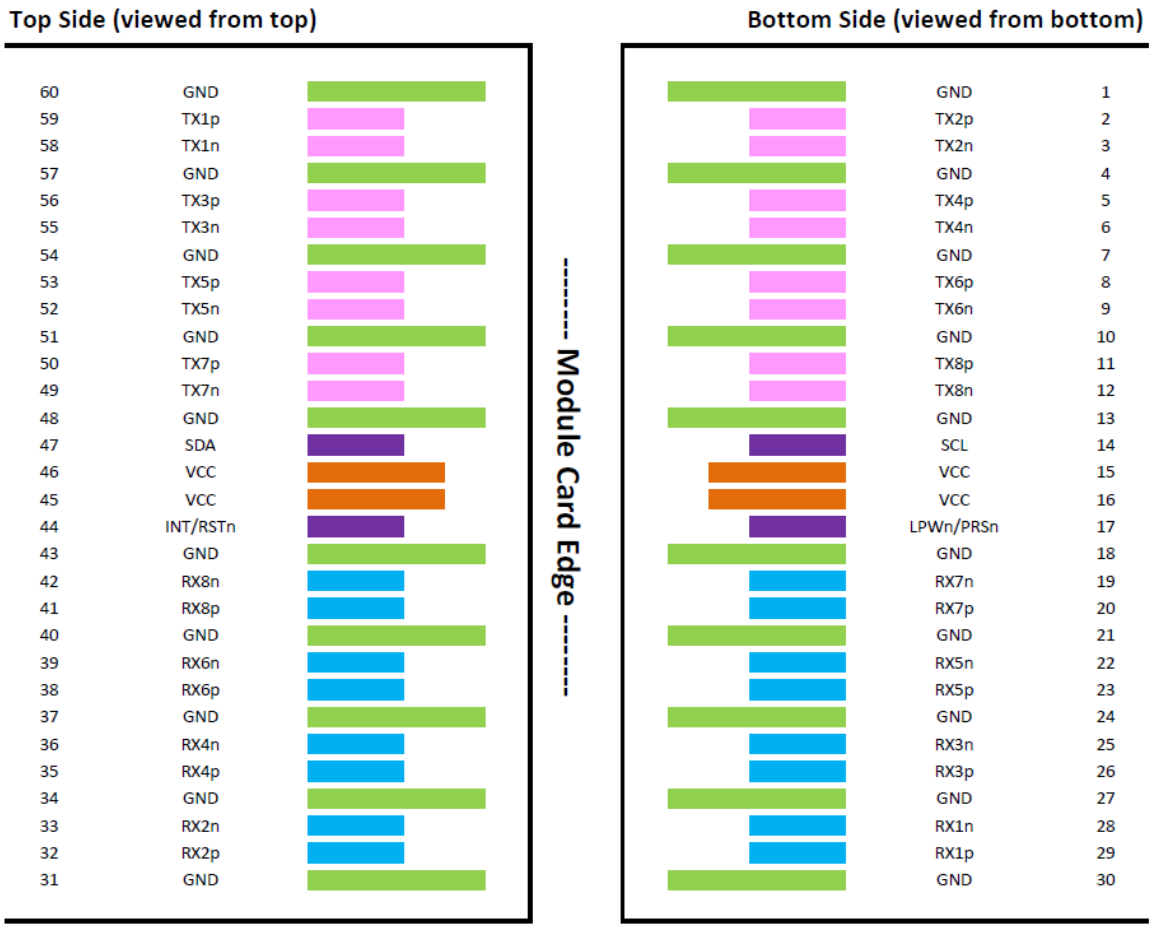


Figure 55: OSFP module pinout

8.2 Pin Descriptions

Table 8-1: OSFP module signal descriptions

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 8.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 8.5.2section
VCC	power	3.3V power for module. Each pin provides 1.5 Amps for a total of 6 Amps (19.8 Watts)
GND	ground	Module Ground. Logic and power return path.

8.3 Pin List

Table 8-2: OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

8.4 High-Speed Signals

The high-speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in either 400GAUI-8 or dual CAUI-4 modes depending on the capability of the host ASIC.

400GAUI-8 mode provides 8 differential lanes using PAM4 signaling operating at 26.5625 GBaud. This results in 8 lanes of 50Gb/s for a total of 400Gb/s. This mode allows connection to PMD configurations of 1x400G, 2x200G, 4x100G or 8x50G.

Dual CAUI-4 mode provides 8 differential lanes using NRZ signaling operating at 25.78125 GBaud. This results in 8 lanes of 25Gb/s for a total of 200Gb/s. This mode allows connection to PMD configurations of 2x100G, 4x50G or 8x25G.

The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd and CEI-56G-VSR-PAM as defined in OIF-CEI-04.0 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

The lane assignments in Table 8-3 shall be used for the different PMD configurations.

Table 8-3: High-speed signal lane mapping

<table>
<tr><th rowspan="2">PMD Configuration</th><th colspan="8">Transmit and Receive Lane Assignments</th></tr>
<tr><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th></tr>
<tr><td>1x400G (PAM4)</td><td colspan="8">Port 1</td></tr>
<tr><td>2x200G (PAM4)
2x100G (NRZ)</td><td colspan="4">Port 1</td><td colspan="4">Port 2</td></tr>
<tr><td>4x100G (PAM4)
4x50G (NRZ)</td><td colspan="2">Port 1</td><td colspan="2">Port 2</td><td colspan="2">Port 3</td><td colspan="2">Port 4</td></tr>
<tr><td>8x50G (PAM4)
8x25G (NRZ)</td><td>Port 1</td><td>Port 2</td><td>Port 3</td><td>Port 4</td><td>Port 5</td><td>Port 6</td><td>Port 7</td><td>Port 8</td></tr>
</table>

8.5 Low-Speed Signals

There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals. LPWn/PRSn and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

8.5.1 SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be 2.2k ohms to 4.7k ohms.

This 2-wire interface supports 4 different bus speeds:

- Standard-mode (Sm) ≤ 100 kbit/s
- Fast-mode (Fm) ≤ 400 kbit/s
- Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- High-speed mode (Hs-mode) ≤ 3.4 Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported I2C

speed the module allows (Upper Page 2, byte 83h). The host may then choose to use a faster I2C speed by setting register (Lower Page 0, byte 50h) provided it is within the supported range. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Standard-mode, Fast-mode, Fast-mode Plus and High-speed mode as defined in the I^2C-bus specification and user manual.

8.5.2 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure *57* enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 56 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

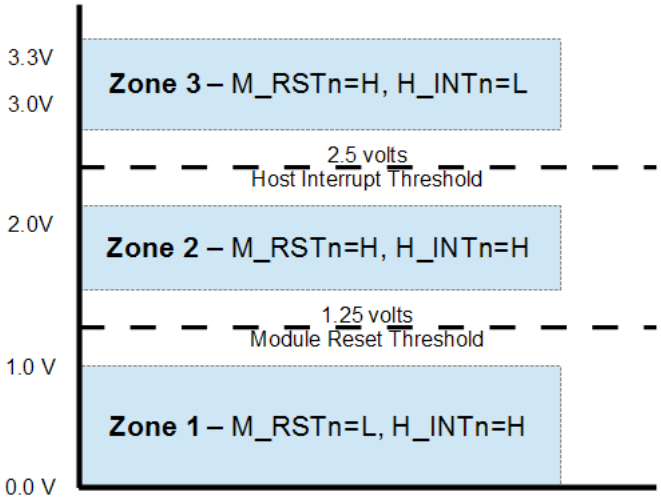


Figure 56: INT/RSTn voltage zones

- Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INTn=High). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 8-4.
- Zone 2 – Normal operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INTn=High). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 8-4.
- Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INTn=Low). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 8-4.

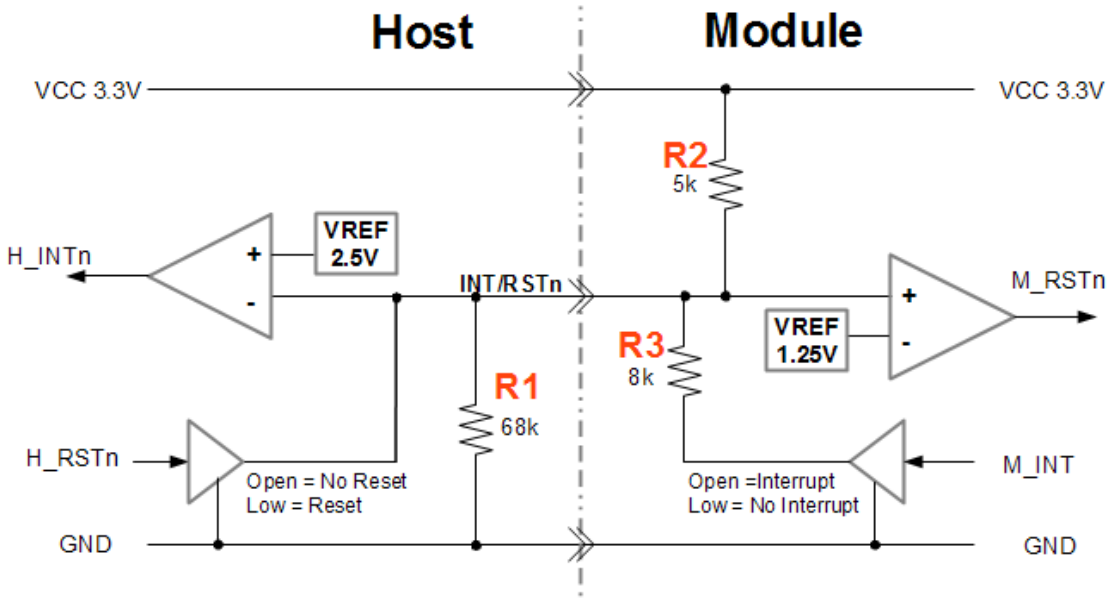


Figure 57: INT/RSTn circuit

Table 8-4: INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INTn	2.500	2.475	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

8.5.3 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 59 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 58 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

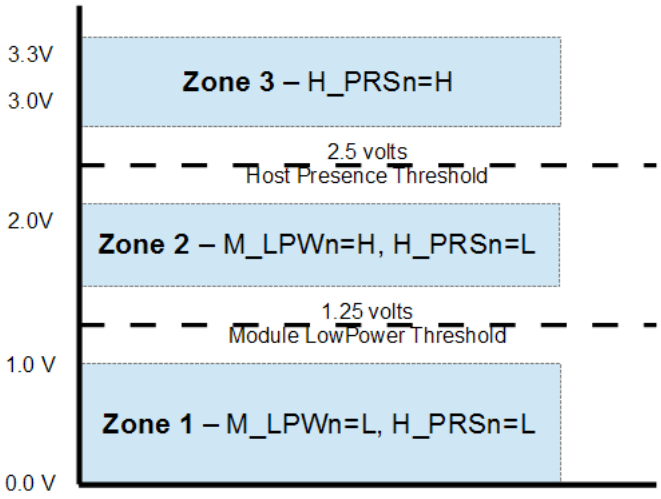


Figure 58: LPWn/PRSn voltage zones

- Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 8-5.
- Zone 2 – High Power mode – Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 8-5.
- Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 8-5.

Module Removal – If the module is being unplugged and LPWn/PRSn loses contact then the pull-down resistor on the module will assert Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp in Table 8-6. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level then 3.3V LVCMOS is preferred.

For very low cost modules, such as DAC, the voltage comparator on the module can be omitted and the LPWn/PRSn pin is tied to GND in the module. This type of module can only be used for low power mode (Power Class 1).

OSFP does not provide a dedicated transmitter disable pin. This function is provided by the TX Disable register via the I2C interface. If a fast hardware shut down is needed then the LPWn signal can be used to shut down the transmitter output and other functions.

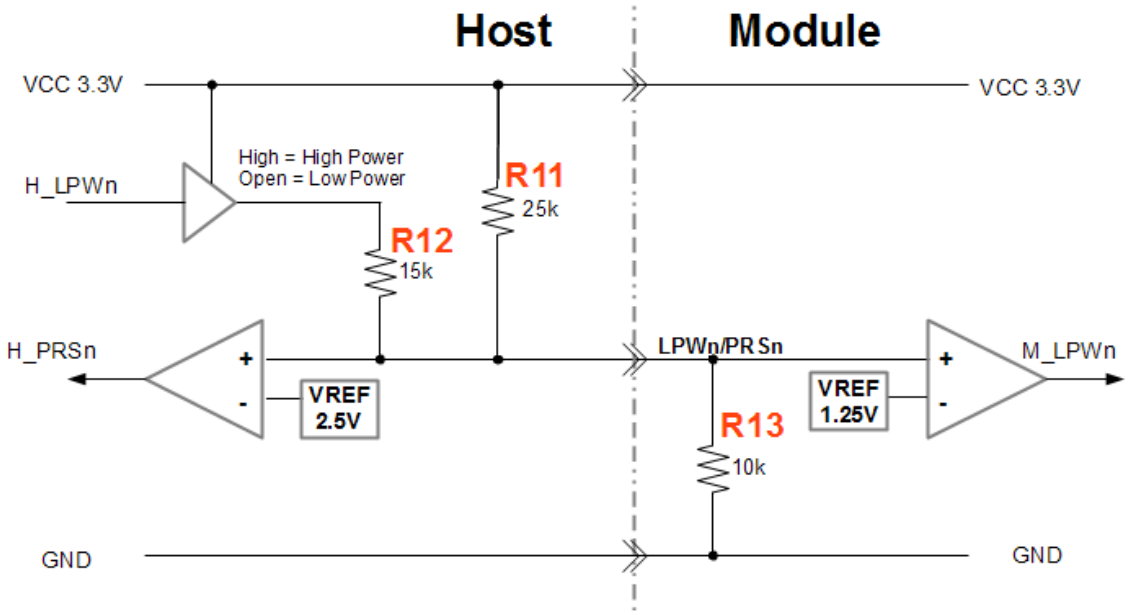


Figure 59: LPWn/PRSn circuit

Table 8-5: LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

8.6 Power

+3.3V power is delivered to the module via 4 power pins (VCC). These 4 power pins shall be connected together on the module and also together on the host. Each power pin allows up to 1.5 Amps for a total of 6 Amps. This enables a potential maximum of up to 19.8 Watts of power to the module.

The specification of the module power is in accordance with methods defined by SFF-8679 Rev 1.7 section 5.5. There are 5 power classes defined as shown in Table 8-7. Power Class 1 is the default low power mode for modules in reset or low power mode as controlled by the M_RSTn and M_LPWn signals. The module must transition to Power Class 1 when M_LPWn (low power mode) or M_RSTn (reset) are asserted. The module must also disable transmitters when M_LPWn or M_RSTn are asserted. Power Classes 2, 3, 4, and 5 are the high power modes for modules that have been enabled via deassertion of both M_RSTn and M_LPWn. The host may also read the module power class register (Upper Page 0, byte 83h) to know the power class of the module before or after enabling high power modes. The module shall not exceed the power class it identifies for itself.

The specifications of Table 8-6 and Table 8-7 are for the combined power of all 4 power pins. The measurement location for these specifications is at the OSFP connector VCC pins on the host board.

Table 8-6: OSFP power specification

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Host power supply voltages including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (1)	I_didt			100	mA/µs
High power mode to Low power mode transition time	T_hplp			200	µs

(1) The specified Inrush and Discharge Current (I_didt) limit must not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power and high-power to low-power.

Table 8-7: OSFP power classes

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Power Class 1 module (low power mode – M_LPWn or M_RSTn asserted)					
Power consumption	P_1			2	W
Instantaneous peak current at hot plug	Icc_ip_1			800	mA
Sustained peak current at hot plug	Icc_sp_1			667	mA
Steady state current (2)	Icc_1		606	638	mA
Power Class 2 module (high power mode)					
Power consumption	P_2			4	W
Instantaneous peak current at high power enable	Icc_ip_2			1600	mA
Sustained peak current at high power enable	Icc_sp_2			1333	mA
Steady state current (2)	Icc_2		1212	1276	mA
Power Class 3 module (high power mode)					
Power consumption	P_3			8	W
Instantaneous peak current at high power enable	Icc_ip_3			3200	mA
Sustained peak current at high power enable	Icc_sp_3			2667	mA
Steady state current (2)	Icc_3		2424	2552	mA
Power Class 4 module (high power mode)					
Power consumption	P_4			12	W
Instantaneous peak current at high power enable	Icc_ip_4			4800	mA
Sustained peak current at high power enable	Icc_sp_4			4000	mA
Steady state current (2)	Icc_4		3636	3828	mA
Power Class 5 module (high power mode)					
Power consumption	P_5			16	W
Instantaneous peak current at high power enable	Icc_ip_5			6400	mA
Sustained peak current at high power enable	Icc_sp_5			5333	mA
Steady state current (2)	Icc_5		4848	5104	mA

(2) Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

8.6.1 Power Filter

Figure 60 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter should be met.

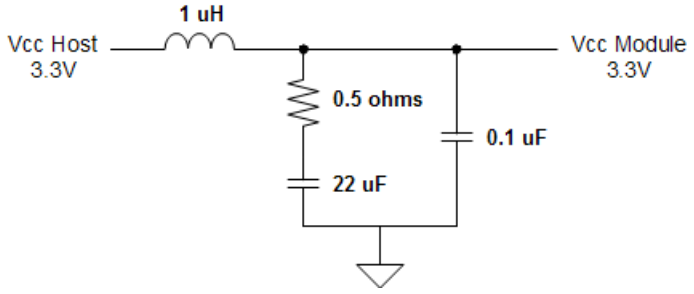


Figure 60: Host board power filter circuit

8.6.2 Power Electronic Circuit Breaker (optional)

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

8.7 OSFP Host Board and Module Block Diagram

Figure 61 is an example block diagram of the host board's connections to the OSFP module.

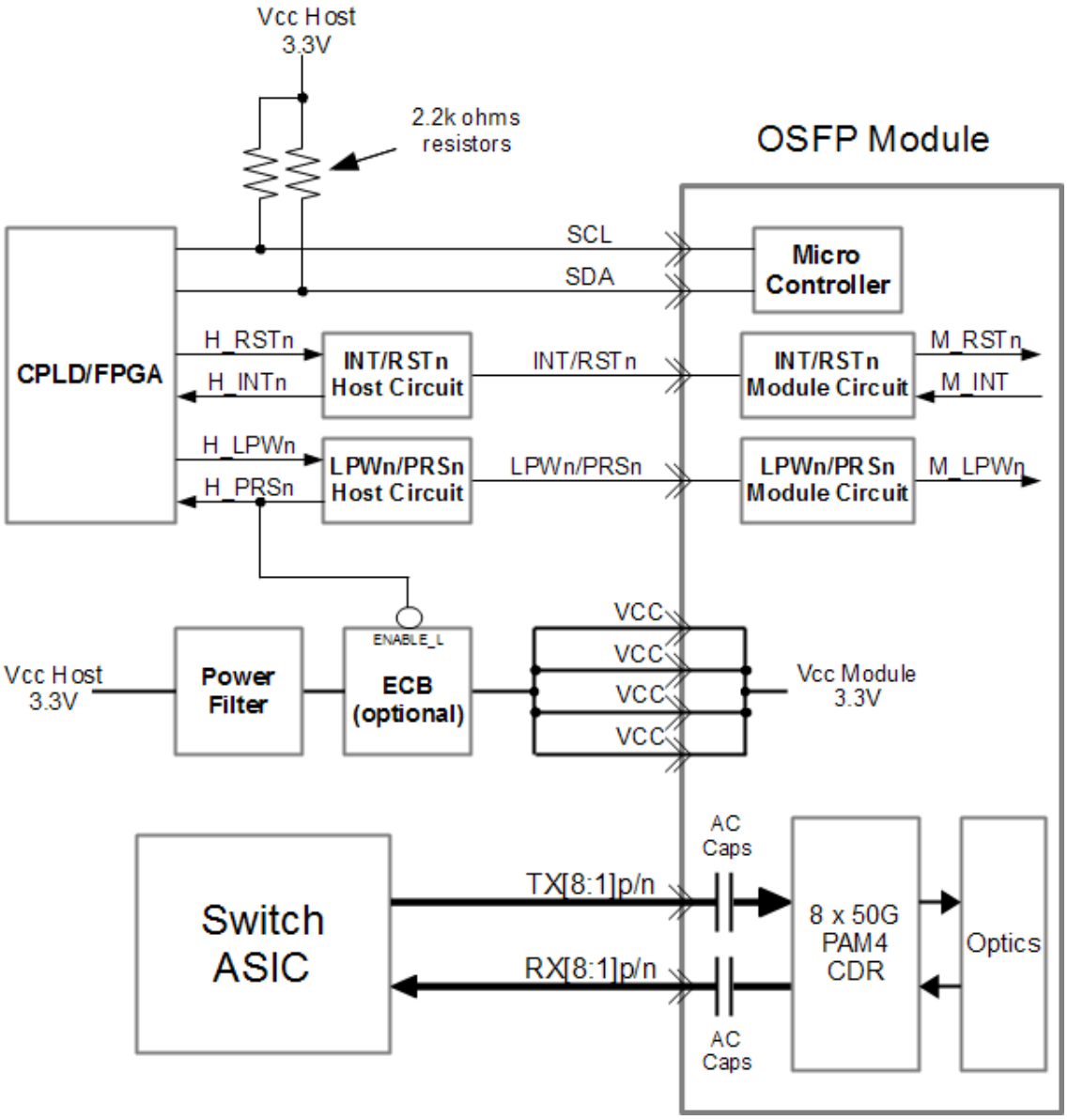


Figure 61: Host board and Module block diagram

8.8 Electrostatic Discharge (ESD)

Where ESD performance is not otherwise specified, the OSFP module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

The OSFP module and host high-speed signal, low-speed signal and power contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

Appendix A. OSFP Module LED (Informative)

A.1 LED Indicator and its Scheme

An OSFP module may have one or more LEDs at the front for use as a status indicator. In cases where a single LED is used for status indication of a multi-channel OSFP module, a green/yellow bi-color LED is recommended. In such case, the LED should light solid green when all channels of the module are operational and solid yellow when all channels are disabled. In cases where some channels are operational and some have fault conditions, a repeating pattern of LED flashing as outlined in Table A-1 is recommended.

Table A-1: Suggested OSFP LED signaling scheme for multiple channel modules

LED Status	Indication
On for 0.22 seconds	Green indicates channel 1 operational; Yellow indicates channel 1 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
On for 0.22 seconds	Green indicates channel 2 operational; Yellow indicates channel 2 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
…. Pattern repeats to final (*n*th) port	…
LED off for 1.76 seconds	Long pause for clear separation before pattern repeats from the beginning.